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Instruction Manual



JOHN FLUKE mfg. co., inc.
SEATTLE WASHINGTON



JOHN FLUKE MFG. CO., INC.

P. O. Box 43210
Mountlake Terrace, Washington 98043



MODEL 1953A COUNTER-TIMER

Rev. 1 - 12/75

Rev. 2 - 2/77

Rev. 6/77

WARRANTY

The JOHN FLUKE MFG. CO., INC.* warrants each instrument manufactured by them to be free from defects in material and workmanship. Their obligation under this Warranty is limited to servicing or adjusting an instrument returned to the factory for that purpose, and to making good at the factory any part or parts thereof; except tubes, fuses, choppers and batteries, which shall, within one year after making delivery to the original purchaser, be returned by the original purchaser with transportation charges prepaid, and which upon their examination shall disclose to their satisfaction to have been thus defective. If the fault has been caused by misuse or abnormal conditions of operations, repairs will be billed at a nominal cost. In this case, an estimate will be submitted before work is started, if requested.

If any fault develops, the following steps should be taken:

1. Notify the John Fluke Mfg. Co., Inc.,* giving full details of the difficulty, and include the Model number, type number, and serial number. On receipt of this information, service data or shipping instructions will be forwarded to you.
2. On receipt of the shipping instructions, forward the instrument prepaid, and repairs will be made at the factory. If requested, an estimate will be made before the work begins, provided the instrument is not covered by the Warranty.

"The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to, any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. Fluke shall not be liable for any special, incident or consequential damages."

SHIPPING

All shipments of John Fluke Mfg. Co., Inc.* instruments should be made via United Parcel Service or "Best Way"*** prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT

The instrument should be thoroughly inspected immediately upon receipt. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument fails to operate properly, or is damaged in any way, a claim should be filed with the carrier. A full report of the damage should be obtained by the claim agent, and this report should be forwarded to John Fluke Mfg. Co., Inc.* Upon receipt of this report, you will be advised of the disposition of the equipment for repair or replacement. Include the model number, type number, and serial number when referring to this instrument for any reason.

The John Fluke Mfg. Co., Inc.* will be happy to answer all application questions which will enhance your use of this instrument. Please address your requests to: JOHN FLUKE MFG. CO., INC., P.O. Box 43210, MOUNTLAKE TERRACE, WASHINGTON 98043*.

* For European customers: FLUKE (Nederland) B.V.
 Ledeboerstraat 27
 Tilburg, Netherlands

** For European customers, Air Freight prepaid.

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Section 1

Introduction & Specifications

1-1. INTRODUCTION

1-2. The Fluke Model 1953A is a universal, 0-to-125 MHz digital counter/timer capable of precisely measuring frequency, frequency ratio, period, time interval and total events. Each measurement function is switch selectable and uses any of six sampling ranges, also switch selectable. Measurement results are displayed by a nine-digit readout, with overflow indication and leading-zero suppression. Frequency is displayed in units of either kHz or MHz; time in units of μ s, ms, or s. The unit also features a self-check function and selection of automatic or manual measurement cycle triggering. Signal input is via BNC connectors.

1-3. The Model 1953A has three input channels designated A, B, and C. Channels A and B are the main input channels. Each is provided with a trigger-level control and signal conditioning switches. Channel C is provided for use with one of three optional, plug-in prescalers. The prescalers extend the measuring capability of the unit to 520 MHz, 1 GHz and 1.25 GHz respectively.

1-4. The trigger-level controls for channels A and B allow the operator to select a preset trigger level (OV dc), or to vary the level at which the input signal will trigger the counter. Two light emitting diode (LED) indicators operate in conjunction with each level control to indicate whether the input signal is more positive or more negative than the selected trigger level. The three conditioning switches allow the operator to select positive or negative slope triggering, ac or dc coupling, and X1 or X10 attenuation of the input signal.

1-5. Each measurement cycle is triggered by a reset signal. The reset signal can be automatically and continuously generated (at an adjustable rate), manually generated (at an adjustable rate), manually generated (by pushbutton switch) once for each measurement cycle desired, or externally generated (optional). The external reset signal is in-

troduced to the 1953A by way of a pin on an optional rear panel connector and may be either manually or automatically generated.

1-6. The front panel display on the 1953A consists of a nine-digit readout, plus one overflow and five measurement unit annunciators (indicators). The readout has leading-zero suppression for all but the right-most digit (the least significant digit). The decimal point and the unit annunciators are controlled by the selected function and the selected range.

1-7. The self-check function provides a convenient method of verifying the operation of the 1953A and is very useful during troubleshooting. During this function the counter automatically selects the 10 MHz output of the internal frequency standard to be the input signal for the digital counter circuits. A valid readout for each of the six selected ranges verifies proper digital operation. This function does not, however, verify the accuracy of the unit. Since the internal frequency standard is being used as the time base as well as the input signal, detection of inaccuracy in the internal frequency standard is not possible. In addition, when the self-check function is selected and the manual reset switch is depressed, every display LED segment that is operating properly will illuminate.

1-8. Several options are available with the 1953A. Each is listed by option number and name in Table 1-1. A detailed description of each option is included in Section 6, Options and Accessories.

1-9. The Model 1953A is designed as a bench-top instrument. However, an Accessory Rack Mounting Kit (part number of Kit without slides is M00-200-622 that for Kit with slides is M00-200-626) is available that will permit the unit to be mounted in a standard 19-inch equipment

rack. Input power requirements are 100, 120, 220 or 240V ac ± 10 percent, 50 to 400 Hz, 30W. The input voltage is selectable by positioning a printed pcb in the power receptacle to display the desired voltage in the viewing port.

1-10. SPECIFICATIONS

1-11. The pertinent specifications for the Model 1953A are listed in the following Table, 1-2. Physical dimensions of the unit are shown in Figure 1-1.

Table 1-1. Available Options

OPTION	NAME	INSTALLATION	
		FACTORY	FIELD SERVICE CENTER
-02	PARALLEL DATA OUTPUT UNIT (DOU)	YES	YES
-04	TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)	YES	NO
-05	EXTERNAL TIMEBASE MULTIPLIER	YES	NO
-07	520 MHz PRESCALER	YES	NO
-10	OVEN-STABILIZED TIMEBASE	YES	NO
-11	BASIC REMOTE CONTROL UNIT (RCU)	YES	NO
-12	FULL REMOTE CONTROL UNIT (RCU)	YES	NO
-13	1000 MHz PRESCALER	YES	NO
-14	1250 MHz PRESCALER	YES	NO
-15	IEEE STANDARD INTERFACE	YES	NO
-16	REAR PANEL INPUTS	YES	NO
-20	SUPERIOR OVEN-STABILIZED TIMEBASE	YES	NO

Table 1-2. Model 1953A Specifications (Continued)

FREQUENCY MEASUREMENTS

Range: 0 to 125 MHz (dc coupled) 5 Hz to 125 MHz (ac coupled) Optional prescalers to 1250 MHz (see options -07, -13, -14)

Gate Time: 0.1 ms to 10s in 6 decade steps (prescaled input increases gate time by a factor of 4 or 8)

Resolution: 0.1 Hz at 10s gate time to 10 kHz at 0.1 ms gate time.

Accuracy: Timebase accuracy ± 1 count

Readout: kHz or MHz automatically displayed with decimal point

RATIO MEASUREMENTS

Displays: f_1/f_2 , where f_1 and f_2 are applied at the two input channels, A and B, respectively

RANGE

f_1 : 0 to 120 MHz (dc coupled), 5 Hz to 120 MHz (ac coupled)

f_2 : 0 to 25 MHz (dc coupled), 5 Hz to 25 MHz (ac coupled)

Accuracy: ± 1 count of signal on input A + trigger error of signal on input B*

Readout: Decimal point without unit annunciation

PERIOD MEASUREMENTS

Range: 0 to 25 MHz (dc coupled), 5 Hz to 25 MHz (ac coupled)

Periods Averaged: 1 period to 10^5 periods

Frequency Counted: 10 MHz

Resolution: 1 ps at 10^5 periods to $0.1 \mu\text{s}$ at 1 period

Accuracy: Timebase accuracy ± 1 count + trigger error of signal on input A*

Readout: ms or μs automatically displayed with decimal point

TIME INTERVAL MEASUREMENT

Range: $0.1 \mu\text{s}$ to 10^7s

Input: Channels A and B; common or separate

Resolution: $0.1 \mu\text{s}$ to 10 ms in 6 decade steps

Accuracy: ± 1 count + timebase accuracy + trigger error**

Readout: ms or s automatically displayed with decimal point

TOTALIZE MEASUREMENT

Totalizing: A gated by B

Range: 0-125 MHz (dc coupled), 5 Hz-125 MHz (ac coupled)

SENSITIVITY

Channel A

Sinewave: 30 mV rms from dc to 75 MHz increasing to 50 mV at 125 MHz

Pulse: 100 mV pulse amplitude with minimum pulse width of 10 ns

Table 1-2. Model 1953A Specifications (Continued)

Channel B

Sinewave: 30 mV rms from dc to 25 MHz

Pulse: 100 mV, with minimum pulse width of 50 ns

Channel C (Prescaled): 15 mV from 50 MHz to 520 MHz (AGC) (option -07). 15 mV from 50 MHz to 1000 MHz (options -13 or -14), increasing to 30 mV at 1250 MHz (option -14 only)

INPUT IMPEDANCE

Channel A or B: 1 M Ω in parallel with 30 pF max

Channel C (Prescaled): 50 Ω nominal, VSWR 2:1 max when not limiting

Dynamic Range w/o Limiting: -3.5 to +3.5 V (Channel A and B) 1V rms (Channel C)

Impedance in Limiting Condition: 120 k Ω in parallel with 75 pF (Channel A and B). VSWR less than 3:1 (Channel C)

ATTENUATOR

Channel A and B only: Sensitivity is decreased by a factor of approximately 10 in the X10 position

SLOPE

Channel A and B only: Front panel slide switch selects positive or negative slope triggering

TRIGGER LEVEL

Channel A and B only: Front panel control has ± 1 V range when attenuator is in X1 position, and ± 10 V in the X10 position. Preset position is fully counter-clockwise

TIMEBASE

	Standard	-04 Option	-10 Option	-20 Option
Frequency:	10.00 MHz	10.00 MHz	10.00 MHz	10.00 MHz
Aging Rate: (constant temp)	$< \pm 3 \times 10^{-7}/\text{mo}$	$< \pm 3 \times 10^{-7}/\text{mo}$	$< \pm 1 \times 10^{-7}/\text{mo}$	$< \pm 1.5 \times 10^{-8}/\text{mo}$
Temperature Stability:				
0°C -50°C	$< \pm 2 \times 10^{-6}$	$< \pm 5 \times 10^{-7}$	$+1 \times 10^{-8}$	$< \pm 2 \times 10^{-10}/^{\circ}\text{C}$
20°C -30°C	$\pm 5 \times 10^{-7}$ typ	$\pm 2 \times 10^{-7}$ typ	$\pm 3 \times 10^{-9}$ typ	$+5 \times 10^{-10}/\text{day}$
Line Voltage: (+10% change)	$< \pm 1 \times 10^{-7}$	$< \pm 5 \times 10^{-8}$	$< \pm 3 \times 10^{-9}$	$< \pm 1 \times 10^{-9}$
Warm Up Time (to 1×10^{-8})	—	—	20 min	20 min

**Trigger error of channels A or B is less than $\pm 0.3\%$ of one period $\div$ periods averaged for signals with better than 40 dB signal to noise ratio and 100 mV rms amplitude*

***Trigger error in time interval mode is less than $\pm 0.0025\%$ signal slope (V/ μ s) in μ s*

EXTERNAL TIMEBASE INPUT

Frequency Required: 10 MHz

Sensitivity: 250 mV rms

Impedance: 1 M Ω , 20 pF

Dynamic Range w/o Limiting: 5V peak to peak

Input Impedance during Limiting: 10 Ω in parallel with 30 pF

DISPLAY

9-digit LED display incorporating large 7-segment characters. Full leading zero suppression

CYCLE RATE:

When in the "CONT" mode, the time interval between

successive measurements can be varied by means of a cycle rate control between approximately 0.2 and 2.0 s. "Reset" button clears display and activates a new measurement

RESET:

In "TRIG" mode the readings may be updated by pushing the "Reset" button or by shorting the external reset pin on the remote control connector to ground. With external reset the display is not cleared.

SELF CHECK:

A timebase-derived 10 MHz signal is internally connected to the counter input

GATE TIME: High true-TTL level output

TIME INTERVAL MARKER:

Low true-TTL level output

OPERATING TEMPERATURE: 0°C to +50°C

STORAGE TEMPERATURE: -40°C to +75°C

POWER REQUIREMENTS:

50-400 Hz; 115/230V $\pm 10\%$ (100V operation available) 30W nominal

DIMENSIONS/WEIGHT

Width:	36.2 cm	(14.25 in)
Height:	8.76 cm	(3.45 in)
Depth:	34.29 cm	(13.5 in)
Weight:	4.32 kg	(9.5 lbs)

OPTIONS**-02 DIGITAL OUTPUT UNIT (PARALLEL)**

Provides BCD TTL outputs from each digit, plus overflow, unit annunciation, decimal point and print command. Write for Fluke Application Bulletin on the 1953A Data Output Option

-04 SUPERIOR TCXO

See time base specifications

-05 TIMEBASE MULTIPLIER

Allows use of external 1, 5 or 10 MHz reference clock (standard unit accepts 10 MHz). This option also permits burst measurements to be made when a "level" signal is available

-10 OVEN-STABILIZED TIMEBASE

Oven is activated whenever instrument is connected to the AC line (see timebase specifications)

-11 BASIC REMOTE PROGRAMMING (PARALLEL)

Allows single-line programming (TTL or contact closure) of range, mode, slope, and reset functions. Allows analog programming of trigger levels, and provides power sense, overflow status, and system ready outputs. Front panel lockout is provided

-12 FULL REMOTE PROGRAMMING (PARALLEL)

Includes all the features of option -11, plus programming of ac/dc coupling, attenuation, separate/common, and digital trigger level. Trigger level of channels A and B is programmable over a +1V to -1V

Table 1-2. Model 1953A Specifications (Concluded)

range (2 BCD digits plus sign), giving a resolution of 1%, and an accuracy of 5% plus 2 mV. Temperature stability is better than 200 μ V/ $^{\circ}$ C. Two analog input/output lines are provided for either checking the D/A performance, or programming via analog levels. Option -12 increases input capacitance to 37 pF max

-15 IEEE STD-488-1975 INTERFACE (SERIAL)

Full remote programming of function, range, and all signal conditioning controls including trigger levels. Directly compatible with IEEE Interface Standard. Data output includes 9 digits of display information, decimal point and exponent for time or frequency units. Front panel lockout is provided. Write for application bulletin covering this option.

-16 REAR INPUTS

2 rear inputs in parallel with A and B front inputs (capacity 85 pF), plus 1 rear input for channel C.

-20 SUPERIOR OVEN-STABILIZED TIMEBASE

Oven is activated whenever instrument is connect-

ed to the AC lines. (see timebase specifications)

1953A-07 INPUT C

Covers frequency range of 50 to 520 MHz, using a scaling ratio of 4. Sensitivity is 15 mV rms (AGC). Maximum allowable input is 5V rms (fuse protected). VSWR less than 2:1 into 50 Ω for levels less than 1V rms

1953-13 INPUT C

Covers 50 to 1000 MHz using a scaling ratio of 8. Sensitivity is 15 mV rms, and maximum allowable input is 5V rms (fuse protected). VSWR less than 2.5:1 (50 Ω) for levels less than 1V rms

1953A-14 INPUT C

Covers 50 to 1250 MHz using a scaling ratio of 8. Sensitivity is 15 mV to 1000 MHz, increasing to 30 mV rms at 1250 MHz. Maximum input 5V rms (fuse protected), and VSWR less than 2.5:1 for levels less than 1V rms

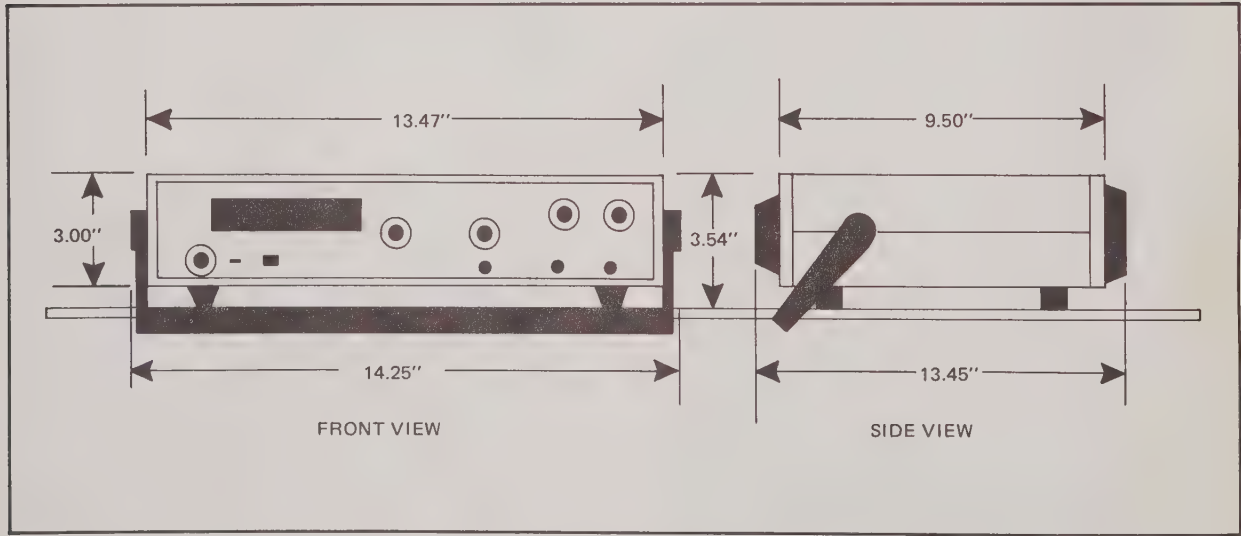


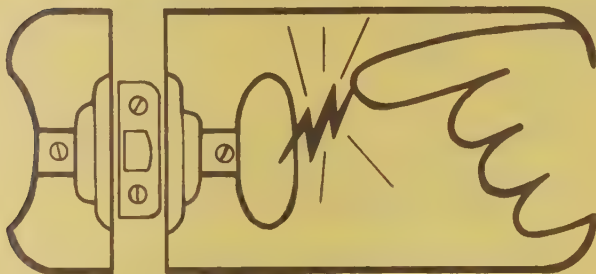
Figure 1-1. Model 1953A Physical Dimensions



static awareness



A Message From
John Fluke Mfg. Co., Inc.



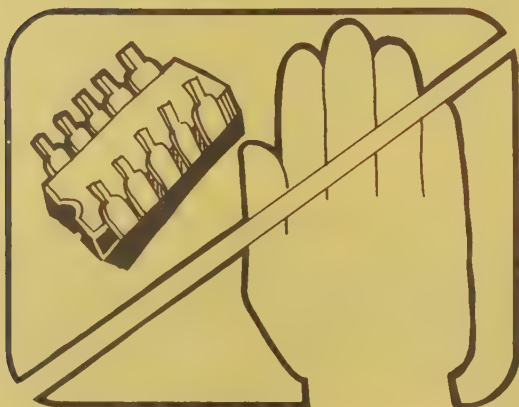
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

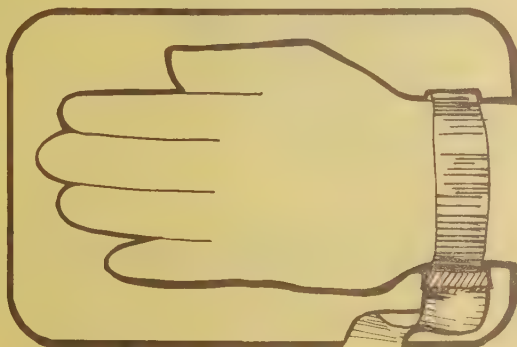
The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol



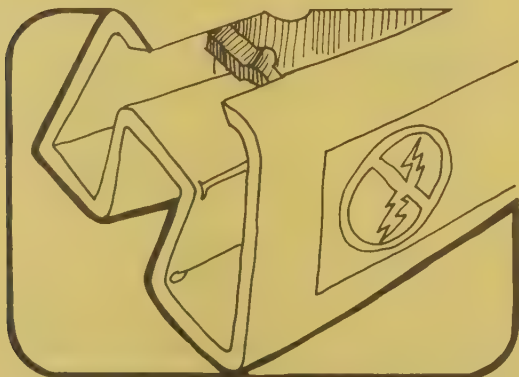
The following practices should be followed to minimize damage to S.S. devices.



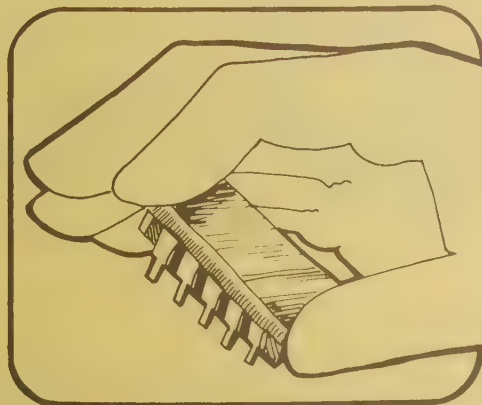
1. MINIMIZE HANDLING



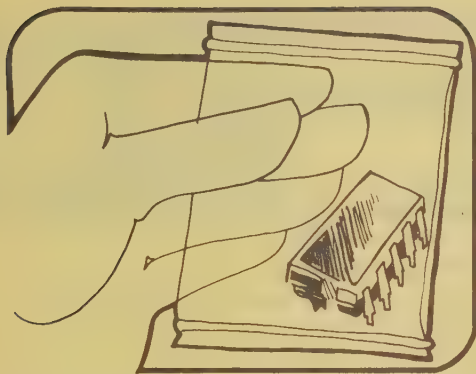
3. DISCHARGE PERSONAL STATIC
BEFORE HANDLING DEVICES



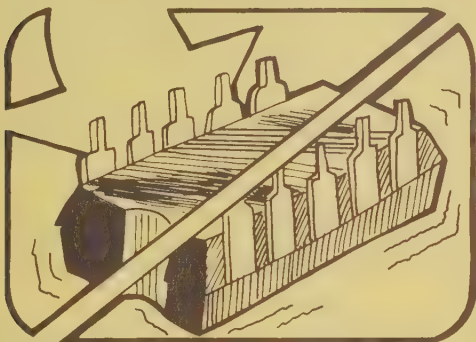
2. KEEP PARTS IN ORIGINAL CONTAINERS
UNTIL READY FOR USE.



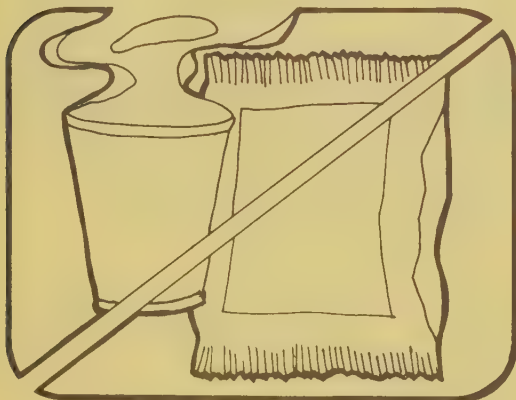
4. HANDLE S.S. DEVICES BY THE BODY



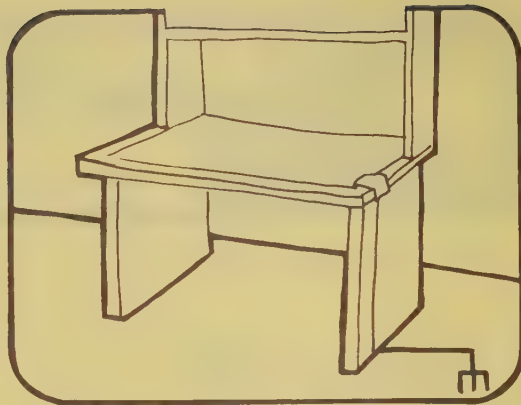
5. USE ANTI-STATIC CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYRAFOAM IN WORK AREA



8. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
9. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
10. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

Anti-static bags, for storing S.S. devices or pcbs with these devices on them, can be ordered from the John Fluke Mfg. Co., Inc.. See section 5 in any Fluke technical manual for ordering instructions. Use the following part numbers when ordering these special bags.

John Fluke Part No.	Bag Size
453522	6" x 8"
453530	8" x 12"
453548	16" x 24"
454025	12" x 15"

Section 2

Operating Instructions

2-1. INTRODUCTION

2-2. This section of the manual contains information regarding installation and operation of the Model 1953A Counter/Timer. It is recommended that the contents of this section be read and understood before any attempt is made to operate the counter. Should any difficulties arise during operation, please contact your nearest Fluke Sales Representative, or contact the John Fluke Mfg. Co., Inc., P.O. Box 43210, Mountlake Terrace, WA 98043; telephone (206) 774-2211. A list of Sales Representatives and their addresses is given in Section 7.

2-3. SHIPPING INFORMATION

2-4. The Model 1953A is packaged and shipped in a protective container. Upon receipt of the equipment, a thorough inspection should be made to reveal any possible shipping damage. Special instructions for inspection and claims are included in the shipping carton.

2-5. If reshipment of the equipment is necessary, the original container should be used. If the original container is not available, a new container can be obtained from the John Fluke Mfg. Co., Inc. Please specify the equipment model number when requesting a new shipping container.

2-6. INPUT POWER

2-7. The Model 1953A can be operated with a line input voltage of either 100, 120, 220 or 240 volts. Before connecting the equipment to primary power visually inspect the present setting of the line switch. It can be read through the clear cover of the combination power receptacle/line switch/fuse holder on the rear panel. Use the following procedure to change to a different setting if required.

- a. Disconnect the line power cord from the receptacle.
- b. Slide the clear cover to the left to cover the power receptacle.
- c. Grasp and pull to the left the handle labeled FUSE PULL till access to the fuse and pcb is clear.
- d. Remove the fuse.
- e. Remove the pcb and position it so the desired voltage figure is on top and to the left, i.e. toward the connector.
- f. Replace the pcb and the fuse. The desired voltage setting should be visible in the opening.
- g. Replace the fuse with the applicable value for the line voltage selected.
- h. Return the holder to its normal position, slide the cover to the right and reinstall the line power cord.

2-8. RACK INSTALLATION

2-9. The 1953A is designed for bench-top use or for installation in a standard 19-inch equipment rack using one of the optional Accessory Rack Mounting Kit (part number M00-200-622) or (M00-200-626). Instructions for installing the unit in the rack mount are supplied with the rack mounting kit.

2-10. OPERATING FEATURES

2-11. The location of all front panel controls, indicators and connectors is shown in Figure 2-1. The name and function of each item shown is given in Table 2-1. The same type of information for those on the rear panel is provided by Figure 2-2 and Table 2-2.

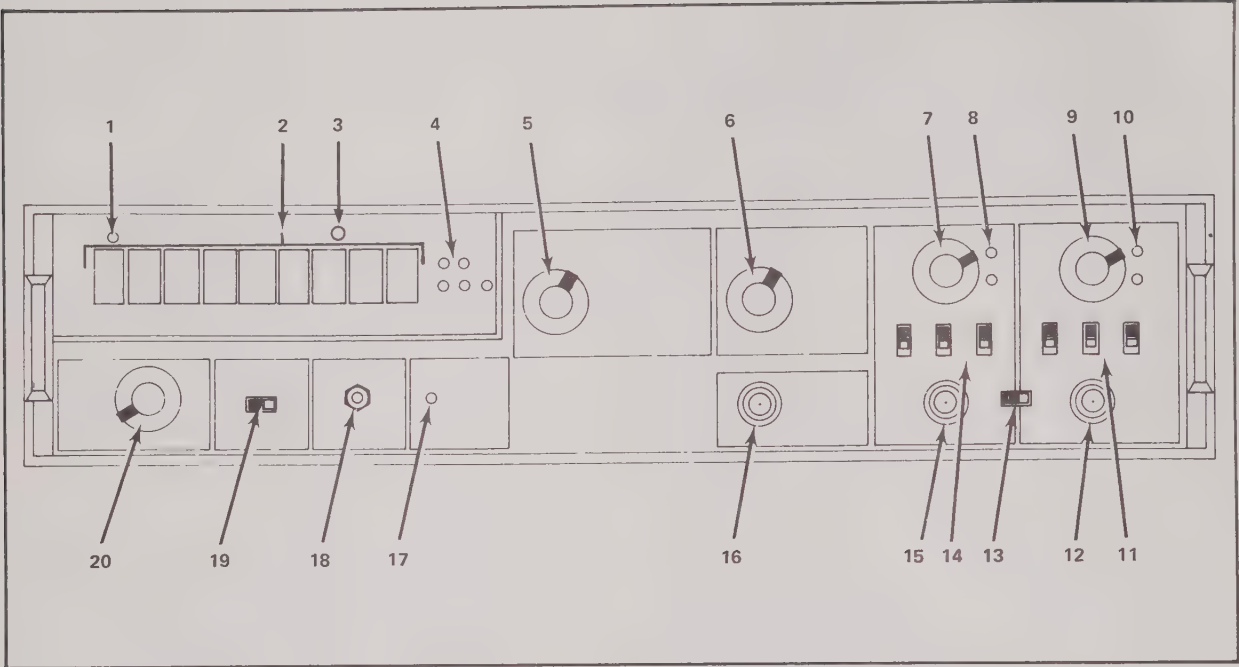


Figure 2-1. Front Panel Controls, Indicators and Connectors

Table 2-1. Front Panel Controls, Indicators and Connectors (Continued)

ITEM NO.	NAME	FUNCTION
1	OVERFLOW Indicator	A LED that lights to indicate that the measurement results readout has exceeded its total display capacity.
2	Measurement Results Readout	Nine-digit readout that digitally displays measurement results. The position of the decimal point, when present, is determined by positions of the RANGE and FUNCTION switches.
3	Remote Indicator	A LED that lights to indicate the instrument is under control of a Remote Device. Active with option -11, -12 or -15 installed.
4	Measurement Unit (Annunciators)	Five LED's, one of which lights, to properly define value displayed. For frequency functions, kHz or MHz annunciator lights; for time functions, ms, us or s annunciator lights; and for ratio, totalize and self-check functions all five remain unlit. (Unit annunciators are controlled by the position of the RANGE and FUNCTION switches).
5	RANGE SWITCH	Selects desired range for selected operating function. Switch positions are interpreted as follows: GATE t Duration of measurement cycle (for frequency functions). PER. AVGD Number of periods averaged (for period functions). T.I. RES. Resolution or value of right-most digit (for time interval function).

Table 2-1. Front Panel Controls, Indicators and Connectors (Continued)

ITEM NO.	NAME	FUNCTION
6	FUNCTION Switch	Selects desired operating function (type of measurement to be made) as follows: FREQ A Enables measurement of frequency of channel A input. FREQ C Enables measurement of frequency of channel C input (channel C is operational only if option -07 or -13 or -14 is installed). FREQ (A/B) Enables measurement of ratio of channel A frequency to channel B frequency. PERIOD A Enables measurement of period of channel A input. T.I. A-B Enables measurement of time interval between start signal at channel A and stop signal at channel B. Start and stop signals may be from separate sources or from same source (see SEP/COM Switch). A GTD. BY B Enables the measurement of total events occurring at channel A during time established by external Gate signal at channel B. (RANGE switch is inoperative during this totalize function). SELF-CHECK Enables check of counter and display circuits; all inputs are disabled, and an internally generated 10-MHz clock signal is counted and displayed.
7	CHANNEL A TRIGGER LEVEL Control	Controls the dc trigger level for the channel A input signal. When set to PRESET (fully ccw), trigger level is 0V dc; when rotated cw, trigger level varies from approximately -1.2V dc (just off PRESET) to +1.2V dc (fully cw).
8	CHANNEL A TRIG STAT + and - (Annunciators)	Two LED's that light alternately to indicate when the input signal level is more positive (+) and when it is more negative (-) than the selected trigger level.
9	CHANNEL B TRIGGER LEVEL Control	Same as item 7, but for channel B.
10	CHANNEL B TRIG STAT + and - (Annunciators)	Same as item 8, but for channel B.
11	CHANNEL B Input Signal Conditioners	Three slide switches that select trigger slope, coupling, and attenuation for channel B input signal. SLOPE Switch Selects either positive or negative-going slope of input (+/-)

Table 2-1. Front Panel Controls, Indicators and Connectors (Concluded)

ITEM NO.	NAME	FUNCTION
		signal to be used to trigger counter.
	Coupling Switch . . . (AC/DC)	Selects either ac (capacitive) or dc (direct) coupling for input signal.
	ATTEN Switch . . . (X1/X10)	Selects either no attenuation (X1) or approximately 20-dB attenuation of input signal voltage (For larger input signals. This allows TRIGGER LEVEL controls to adjust trigger level from approximately -12V dc to +12V dc).
12	CHANNEL B Input Connector	A BNC connector used to connect an input signal to channel B.
13	SEP/COM Switch	Sets up signal input connectors to receive either separate signals or a common signal, as desired. When set to COM channel A input is connected to channel A and channel B pre-amplifiers; when set to SEP, they are isolated.
14	CHANNEL A Input Signal Conditioners	Same as item 11, but for channel A.
15	CHANNEL A Input Connector	Same as item 12, but for channel A.
16	CHANNEL C Input Connector	Same as item 12, but for channel C (Channel C connector is supplied only with options -07, -12 and -14).
17	GATE Indicator	A LED that lights to indicate that a measurement cycle is being executed.
18	RESET Push-Button	Resets readout to zero and initiates new measurement cycle.
19	MODE Switch (CONT/TRIG)	Selects either automatic or manual triggering of measurement cycles. When switch is set to CONT, measurement cycles are automatically and continuously initiated at adjustable repetition rate; when switch is set to TRIG, single measurement cycle is initiated each time RESET switch is pressed or whenever ground is applied to external reset pin on optional REMOTE CONTROL connector on rear panel. (Automatic triggering is locked out in TRIG position, but manual and external triggering remain operational in CONT position).
20	POWER/CYCLE RATE Control	Adjusts repetition rate of automatic measurement cycle triggering from approximately 0.2 to 2.0 seconds. When rotated to OFF detent (fully ccw), power to unit is turned off. For options -11 and -12 controls the Remote/Local Status. For options -10 and -20 provides standby power to the instrument. With one of each type of option installed (RCU and ovenized timebase) the RCU feature is used and all power control of the instrument will be from the rear panel.

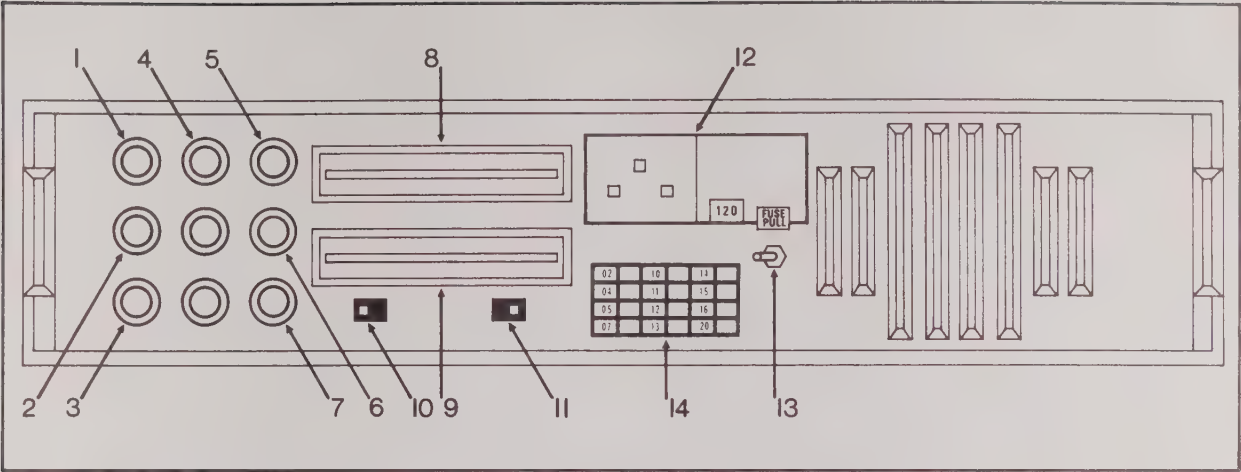


Figure 2-2. Rear Panel Controls and Connectors

Table 2-2. Rear Panel Controls and Connectors (Continued)

ITEM NO.	NAME	FUNCTION
1	CHANNEL A Input Connector	Connector serves as rear panel input to channel A. This is part of Option -16 (see section 6).
2	CHANNEL B Input Connector	Same as 1, but for channel B.
3	CHANNEL C Input Connector	Same as 1, but for channel C, prescaled input. Front panel channel C connector is not installed when rear panel channel C connector is installed (see section 6).
4	MARKER Connector	Provides connection for Marker output signal. This signal is applied to Z-axis input of oscilloscope displaying 1953A input signal. The result is an intensified zone that indicates start-to-stop time of time interval measurement. In agreement with modulation requirements for Z-axis inputs of most oscilloscopes, the pulse is low active (and high, or +5V, when inactive).
5	GATE TIME Connector	Provides connection for Gate Time output signal. This signal is an active high, TTL-compatible pulse generated for duration of measurement cycle.
6	CLOCK OUTPUT Connector	Provides connection for 10 MHz clock signal (internal or external) being used as timebase standard. The output is buffered and is TTL compatible.
7	EXT 10 MHz CLOCK Connector	Provides connection for external 10 MHz clock input signal. Minimum input level required is 100 mV, and input impedance is 1 Megohm.
8	BCD OUTPUT/IEEE ADDRESS Connector	Provides connection, when installed, for BCD parallel output (part of Option -02) or access to IEEE address controls (part of Option -15).

Table 2-2. Rear Panel Controls and Connectors (Concluded)

ITEM NO.	NAME	FUNCTION
9	REMOTE CONTROL Connector	Provides connection when installed, for remote control of 1953A. (This is part of Options -11, -12 and -15).
10	Clock Select Switch	Selects either internal or external clock for use as 1953A timebase standard: INT Selects output of internal clock. EXT Selects external clock connected to Item 7.
11	NORMAL/BURST Select Switch	Installed as part of Option -05 (see Section 6), allows choice of normal signal measurements or RF burst measurements.
12	Input Power Connector	Provides connection for ac input power. Contains Fuse receptacle and selection pcb to select between 100, 120, 220 or 240 input line voltage.
13	REAR PANEL POWER SWITCH	Part of Option -10, -11, -12 and -20. When on, with -10 or -20 installed and neither -11 or -12 installed, provides power to the oven filaments independently of the front panel power switch. When on with -11 or -12 installed, supplies operating power to the instrument, and the Front Panel Power Switch controls the remote/local command. When off disconnects entire unit from mains.
14	OPTION DECAL	Designation of options selected.

2-12. OPERATING NOTES

2-13. The following paragraphs describe various conditions that should be considered before operating the Model 1953A Counter/Timer.

2-14. AC Line Connection

2-15. The input power cord mates with a three-prong, polarized connector. This permits connection to any of the power line voltages described in paragraph 2-6. Ensure that the offset pin is connected to a high-quality earth ground.

2-16. Input Channels A and B

2-17. Input Channels A and B are electrically similar, with bandwidths extending from 0 to 125 MHz for channel A, and 0 to 25 MHz for channel B. The output rise times for channels A and B are 5 ns and 20 ns, respectively. The input impedance of each channel is 1 Megohm. A clamping circuit limits the voltage to the first stage of the input amplifier to $\pm 3.5V$, nominal. When the ATTEN switch is set to X1, the input impedance will decrease sharply to 120 kilohms for that portion of the input signal that exceeds the limit voltage. When the ATTEN switch is set to X10, the input impedance remains at 1 Megohm for all input signal levels.

2-18. The sensitivity of channel A for sine-wave inputs is 30 mV rms minimum from 0 to 75 MHz. The sensitivity gradually decreases to 50 mV rms minimum at 125 MHz. For channel B the sensitivity for sine wave inputs is 30 mV over the entire bandwidth (0 to 25 MHz). For pulse inputs the sensitivity is 100 mV peak-to-peak minimum for both channels with a minimum pulse width of 10 ns for channel A, and 50 ns for channel B.

2-19. Overload protection for input channels A and B permits a maximum signal level of 150V rms, from dc to 1kHz, to be applied to either input without damaging the unit. The maximum allowable input signal level gradually decreases to 5V rms at 125 MHz when the ATTEN switches are set to X1; or to 50V rms, when set to X10.

2-20. SEP/COM Switch

2-21. The SEP/COM switch is used to isolate the A and B inputs when the switch is set to SEP, or to connect channel A input to both channel A and B preamplifiers, when set to COM. The switch is normally left at SEP except in the case of time interval measurements using a single input signal. With the switch set to COM, channel A is used to establish the Start Signal trigger level conditions and channel B is used to establish the Stop Signal trigger level conditions.

2-22. Signal Conditioning

2-23. The signal conditioning features provided for each of the two main input channels (A and B) consist of a TRIGGER LEVEL control, a trigger status indicator (TRIG STAT), and three slide switches. The slide switches condition the input signal before it is used to trigger the counter, by selecting the desired trigger slope (+ or -), coupling (ac or dc) and attenuation (X1 or X10). The TRIGGER LEVEL control is continuously variable from approximately -1.2V to +1.2V dc (with the X1 attenuation selected; selecting the X10 attenuation increases the range of the TRIGGER LEVEL control by a factor of 10). When the control is rotated fully ccw to PRESET, the trigger level will be 0V dc.

2-24. The TRIG STAT indicator consists of two LED's one marked + the other marked -. For sine-wave inputs these LED's indicate the relative trigger level selected. With the TRIGGER LEVEL control set to PRESET (0V dc trigger level), the two LED's will light with equal intensity. If the TRIGGER LEVEL control were adjusted to produce a -0.7V trigger level, as in case 1 of Figure 2-3, the + LED would light more brightly than the -LED. This is due to the fact that the LED's are driven on a complementary basis. With a negative trigger level, the + LED is on for a longer portion of the input waveform than the -LED and thus, appears to be brighter to the eye. For pulse inputs, the LED's fail to indicate relative trigger level since their brightness is related to the relative duty cycle of the waveform. With the pulse input waveform shown in case 2 of Figure 2-3, the -LED would glow more brightly regardless of the trigger level. In case 3, the LED's would have equal intensity, again regardless of the trigger level. However, if the waveform in case 3 were just half the peak voltage of that shown, the STAT TRIG indicators then provide a means of determining the effective range of the TRIGGER LEVEL control. When the TRIGGER LEVEL control is rotated either direction from the midpoint (approx 0V dc), as soon as the trigger level exceeds the peak voltage of the waveform, the corresponding LED will no longer light. This is best seen with pulse inputs, where the transition is sudden; with sine waves the transition is gradual. Very narrow pulses may not light a LED to the point where it can be seen, even though proper triggering of the counter occurs.

2-25. Marker Output

2-26. In the time interval function, a negative-going (low true) pulse is generated at the MARKER connector to provide an indication of the actual time interval being measured. The width of the Marker pulse is variable, depending on the trigger levels selected for channels A and B (Start and Stop signals). When the

input signal is fed to the vertical input of an oscilloscope the marker pulse can be used to drive the Z-axis of the scope and cause the measured portion of the input signal to be intensified. Using this technique, the trigger levels for channels A and B (Start and Stop signals) can be individually adjusted for precise time interval measurements.

2-27. In the frequency A function, the Marker pulse can be used to precisely set the trigger level for channel A. However, the trigger level for channel B must also be adjusted to reset the Marker Generator. This is accomplished by setting the SEP/COM switch to COM adjusting the TRIGGER LEVEL control for channel B so that the intensified zone is terminated shortly after it begins. Then adjust the TRIGGER LEVEL control for channel A to the desired position

2-28. Gate Time Output

2-29. The GATE connector provides a high TTL output while the counter is executing a measurement cycle in any of the available functions. For Frequency A and C functions, the duration of the Gate signal is equal to the Gate time (GATE t) selected by the RANGE switch.

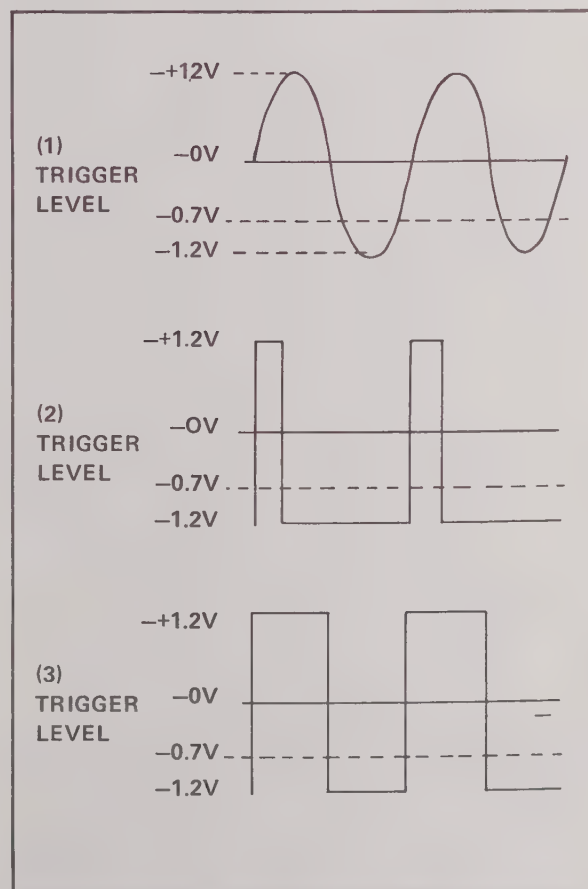


Figure 2-3. Effect of Input Wave Shape on Status Indicators

The signal is intended for use in remote applications; however, it can be used as a scope trigger or an external time gate. The GATE indicator lights for the duration of the Gate signal, plus approximately 100 ms. The extra 100 ms is provided by a pulse stretcher to ensure a sufficient on-time (duty cycle) for the GATE indicator to be seen when the shortest gate times are selected.

2-30. OPERATION

2-31. Turn-On Procedure

2-32. Use of the following procedure is suggested for initial turn-on of the 1953A:

- a. Connect the 1953A to ac power line (Refer to paragraph 2-6).
- b. Turn the CYCLE RATE control cw, off the OFF detent. The front panel display should illuminate.

2-33. Operating Functions

2-34. The following paragraphs describe the self-check frequency, ratio, period, time interval and totalize functions and give the procedures necessary to operate the 1953A for each.

2-35. SELF CHECK

2-36. The self check function is used to verify the digital operation of the 1953A. The frequency of the 10 MHz oscillator is measured to produce a predictable readout for each setting of the RANGE switch. Pressing the RESET switch when the counter is in the SELF CHECK mode causes all digit segments to be illuminated. This provides immediate verification that all segments of the display LED's are operational. This LED check takes effect regardless of the position of the CONT/TRIG switch.

2-37. Use the following procedure to operate the 1953A for the Self Check function:

- a. Turn CYCLE RATE control cw, off the OFF detent.
- b. Set rear panel Clock Select switch to INT.
- c. Set FUNCTION switch to SELF CHECK.
- d. Set CONT/TRIG switch to CONT.
- e. Adjust CYCLE RATE control for desired display period.
- f. Sequentially select each GATE t position of RANGE switch, pausing at each position to verify proper display in readout. (Table 2-3 shows proper display for each GATE t selected.)

Table 2-3. Display For Self Check

GATE	READOUT
0.1 ms	1000
1.0 ms	10000
10 ms	100000
0.1 s	1000000
1.0 s	10000000
10 s	100000000

2-38. FREQUENCY

2-39. Standard frequency measurements from 0 to 125 MHz are made using the frequency A function. The gate times available for each frequency measurement range from 0.1 ms to 10s in six decade steps and are selected by means of the RANGE switch. For a given input signal there will be a RANGE setting (gate time) which will give optimum resolution of the displayed frequency.

2-40. Use the following procedure to operate the 1953A for the frequency A function:

- a. Turn the cycle rate control cw, off the OFF detent.
- b. Set FUNCTION switch to FREQ. A.
- c. Set CONT/TRIG switch to CONT.
- d. Connect input signal to be measured to CHANNEL A input connector.
- e. Adjust CHANNEL A TRIGGER LEVEL control to establish desired trigger conditions. (Normal triggering occurs when both the + and - TRIG STAT indicators are lit.)
- f. Adjust CYCLE RATE control for desired display period.
- g. Set RANGE switch to obtain optimum resolution of the frequency displayed.

2-41. Used with any one of three optional prescalers, the frequency C function increases the frequency measurement capability of the 1953A to frequency ranges extending from 50 MHz to 520 MHz (using Option -07), or from 50 MHz to 1GHz (using Option -13), or from 50 MHz to 1.25 GHz (Using Option -14). Refer to Section 6 for operating instructions for the frequency C function.

2-42. RATIO

2-43. The ratio function is used to measure the frequency ratio of two input signals. One signal is coupled into channel A, the other into channel B. The resolution of the measurement can be increased or decreased by changing the setting of the RANGE switch. Optimum resolution is obtained by insuring that the higher fre-

quency input signal is connected to the CHANNEL A input.

NOTE!

For ratio measurements, the channel B input frequency is limited to 25 MHz maximum.

2-44. Use the following procedure to operate the 1953A for the ratio function:

- a. Turn CYCLE RATE control cw, off the OFF detent.
- b. Set FUNCTION switch to FREQ (A/B).
- c. Set CONT/TRIG switch to CONT.
- d. Set SEP/COM switch to SEP.
- e. Connect the higher of two frequencies to be measured to CHANNEL A input connector.
- f. Connect other frequency to CHANNEL B input connector.
- g. Adjust the CHANNEL A and the CHANNEL B TRIGGER LEVEL controls to establish desired trigger conditions. (Proper triggering occurs when both + and – TRIG STAT indicators are lit.)
- h. Adjust CYCLE RATE control for desired display period.
- i. Set RANGE switch to obtain optimum resolution of ratio displayed.

2-45. PERIOD

2-46. The period function is used to measure the period of input signals with frequencies up to 25 MHz. This function is also intended for use in measuring low frequencies, since a low frequency can be determined with higher resolution through a period measurement than through a direct frequency measurement. The measurement resolution increases with the number of periods used to obtain the average. For example, if the RANGE switch is set to 10^0 (PER AVGD. column), and an input frequency of 1Hz is applied to channel A, the readout will display 1000.0000 ms (resolved to 100 ns). Setting the RANGE switch to 10^1 will cause the display to read 1000.00000 ms (resolved to 10 ns). In the frequency mode, however, with a 1Hz signal and a 10 second gate time the maximum resolution is 0.1 Hz. The setting of the RANGE switch indicates, in powers of ten, the number of periods (cycles) of the input signal that are sampled to produce the final display.

2-47. Use the following procedure to operate the 1953A for the period average function:

- a. Turn CYCLE RATE control cw, off the OFF detent.
- b. Set FUNCTION switch to PERIOD A.
- c. Set CONT/TRIG switch to CONT.
- d. Connect signal to be measured to CHANNEL A input connector.

- e. Adjust CHANNEL A TRIGGER LEVEL control to ensure proper triggering.
- f. Adjust CYCLE RATE control for desired display period.
- g. Set RANGE switch to the PER AVGD. position that provides desired resolution.

2-48. TIME INTERVAL

2-49. With the time interval function, accurate measurements can be made of the time interval between the occurrence of two separate input signals or between two points on a single input signal. In either case, channel A is used to provide a Start signal, and channel B is used to provide a Stop signal. When a single input signal is to provide both the Start and the Stop signals, the SEP/COM switch is set to COM so that both channels A and B receive the same signals. The SEP/COM switch is set to SEP when the Start and the Stop signals are to be provided by separate input signals.

2-50. Accurate pulse width, rise time and fall time measurements can be made with the time interval function. However, their accuracy depends on the trigger levels being set so that the Start and Stop signals occur at precise voltage levels of the input signal. The trigger levels can be visually set using an oscilloscope to display the input signal, while driving the Z-axis of the scope with the Marker signal (available at the rear panel). The measured time interval appears as an intensified zone on the scope trace and can be adjusted using the CHANNEL A and CHANNEL B TRIGGER LEVEL controls. Refer to the discussion of the MARKER Output given earlier in this section under Operating Notes.

2-51. Use the following procedure to operate the 1953A for the time interval function:

- a. Turn CYCLE RATE control cw, off the OFF detent.
- b. Set CONT/TRIG switch to CONT.
- c. Set FUNCTION switch to T.I. A-B.
- d. Set SEP/COM switch to SEP if Start/Stop signals are to be derived from separate input signals, or to COM, if from single input signal.
- e. If separate input signals are used, connect Start signals to CHANNEL A input connector, and the Stop signal to CHANNEL B input connector. If single input is used, connect it to either input connector.
- f. Adjust CHANNEL A and CHANNEL B TRIGGER LEVEL controls to establish desired Start/Stop trigger levels. Use the Marker output in conjunction with an oscilloscope to establish precise trigger levels.
- g. Adjust CYCLE RATE control for desired display period.
- h. Set RANGE switch to the T.I. RES position that provides desired resolution.

2-52. TOTALIZE

2-53. In the totalize function, the 1953A can be used as a gateable totalizer. Each event that occurs at the CHANNEL A input connector is accumulated (totalized) during the time that a signal at the CHANNEL B input connector produces a gate pulse for the accumulator. The CHANNEL B SLOPE switch selects the portion of the channel B waveform that will produce the gate pulse. When the SLOPE switch is in the + position a gate pulse will be produced during the time the input waveform is more positive than the trigger level established for channel B; when in the – position, during the time the input signal is more negative. The RANGE switch is inoperative during this function.

NOTE!

To prevent the enabling edge of the CHANNEL B gate pulse from triggering the counter, the SLOPE switch for Channel A should be set to indicate the active polarity of the Channel A input signal.

2-54. Use the following procedure to operate the 1953A for the totalize function:

- a. Turn CYCLE RATE control cw, off the OFF detent .
- b. Set FUNCTION switch to A GTD. BY B.
- c. Set SEP/COM switch to SEP.
- d. Connect signal to be totalized to CHANNEL A input connector.
- e. Connect signal to be used for gating to CHANNEL B input connector.
- f. Adjust the CHANNEL A and CHANNEL B TRIGGER LEVEL controls to ensure proper triggering. The counter will totalize events on channel A as long as the channel B input is at an active level. In this mode the display will be updated only when the RESET switch is pressed, or when an External Reset signal is activated (no automatic recycling).

NOTE!

If no input signal to Channel B is required or available, the gating of the accumulator can be manually controlled by the CHANNEL B SLOPE switch. Turn the CHANNEL B TRIGGER LEVEL control fully cw. Setting the SLOPE switch for CHANNEL B to – will now gate the accumulator, and the 1953A will totalize. Setting it back to + will inhibit the accumulator, and the totalizing will halt. To resume totalizing, set the SLOPE switch to – again; to start over from zero, momentarily press the RESET switch.

Section 3

Theory of Operation

3-1. INTRODUCTION

3-2. This section of the manual contains a functional block diagram description of the Model 1953A counter. Detailed functional block diagrams are also included. A complete set of schematic diagrams is included in Section 8.

3-3. OVERALL FUNCTIONAL DESCRIPTION

3-4. Figure 3-1 is a simplified block diagram of the 1953A. It shows the major functional elements of the unit. The heart of the 1953A is the accumulator. The accumulator counts the clock pulses applied to it during the gate pulse. It retains this count, until a new measurement cycle is initiated, for use in driving the measurement results readout (nine-digit readout and overflow indicator). The accumulator receives the clock pulses from the function control logic circuits. In three

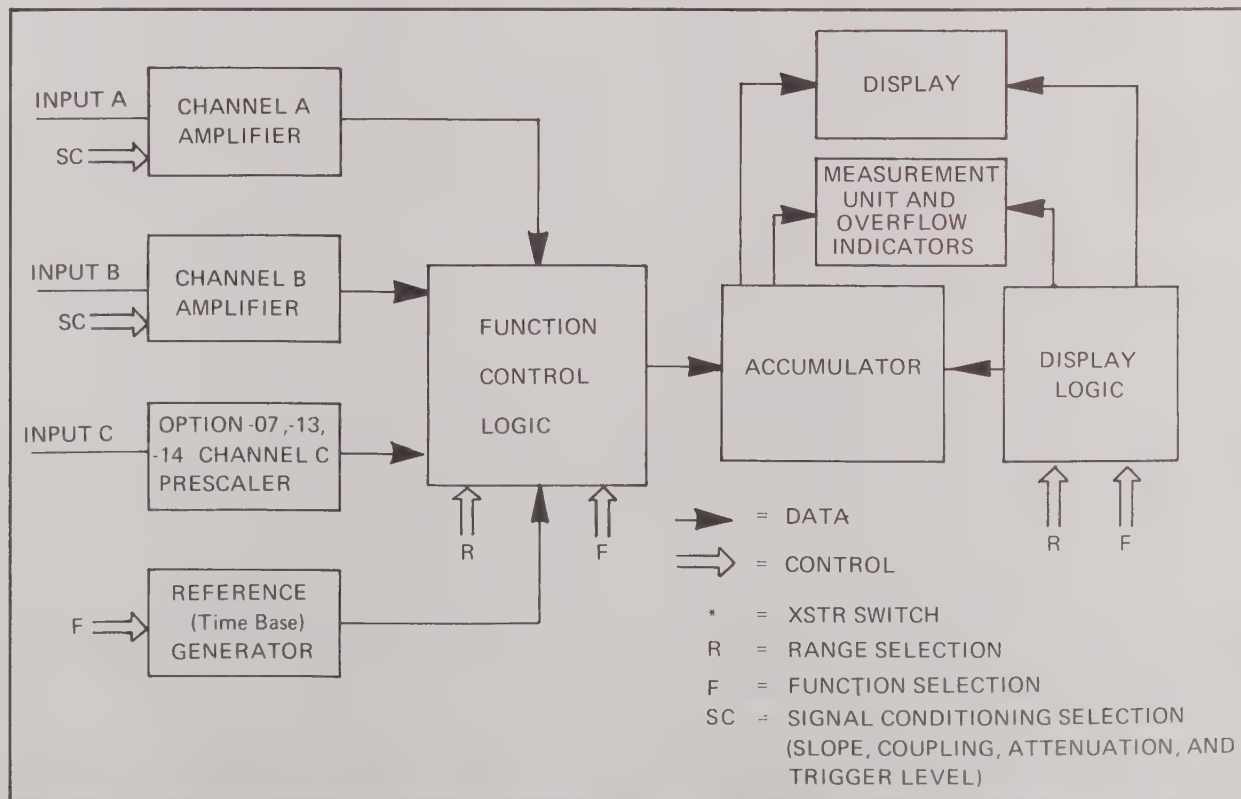


Figure 3-1. Model 1953A, Simplified Block Diagram

functions (Frequency A, Ratio A/B and A Gtd. by B) the clock pulses are fed straight through to the accumulator from channel A for the duration of the gate pulse. Under control of the FUNCTION switch, the function control logic circuits select the sources from which to derive the clock and the gate pulses. Table 3-1 lists sources for each measurement function. The duration of the gate pulse is a function of the RANGE switch. Decimal point location and measurement unit indication are automatically controlled by the RANGE and the FUNCTION switches through the display logic circuits.

Table 3-1. Accumulator Input Signal Summary

FUNCTION SWITCH	CLOCK Derived From	GATE Derived From
FREQ A	Channel A*	Ref. Generator
FREQ C	Channel C	Ref. Generator
FREQ (A/B)	Channel A*	Channel B
PERIOD A	Ref. Generator	Channel A
T.I. A-B	Ref. Generator	Channels A&B
A GTD BY B	Channel A*	Channel B*
SELF CHECK	Ref. Generator	

*Direct feed-through, not derived.

**RANGE switch has no effect on Gate pulse.

3-5. When performing frequency measurements (with FREQ A or FREQ C of the FUNCTION selection), the counter accumulates cycles of the unknown input frequency for a pre-selected time interval termed the gate time. The total number of cycles accumulated is displayed in the readout and converted by the automatic placement of a decimal point into units of kHz or MHz (the units are indicated by the annunciators). There are six gate times available in the 1953A ranging from .1 ms to 10 s in decade steps. These gate times are derived from the 10 MHz reference generator via the associated timebase divider circuitry and are selected by means of the RANGE switch. In channel A frequency measurements the gate times are selected directly from the RANGE, while in channel C prescaled frequency measurements the gate times shown in the RANGE are multiplied by a factor of either four (with Option 07) or eight (with Options -13 and -14).

3-6. Basically, measurements of period or of time intervals involve the counting of periods of the reference timebase during a gate interval derived from an input signal. When performing period measurements on an input signal the counter accumulates period of the 10 MHz reference generator during a gate interval determined by a pre-selected number of periods of the input signal. The number of periods which establish the gate time are selected from the Periods Averaged column of the RANGE, which is scaled in six powers of ten

giving from 1 to 10^5 periods of gating time. Direct period measurements are made when the gate interval is determined by a single period of the input signal, and period average measurements are made when more than one period comprises the gate interval. Since each cycle of the reference frequency has a period of 0.1 μ s, the accumulator actually counts the number of 0.1 μ s periods that occur during the gate time. This number is displayed in the readout and converted by the automatic placement of a decimal point and units annunciation, into units of either microseconds or milliseconds. To make time interval measurements, the counter accumulates cycles of a signal derived from the timebase divider circuitry, during the gate interval. The 10 MHz reference timebase is divided by powers of ten to yield a selection of six reference signals ranging from 10 MHz to 100 Hz. Any of the six frequencies may be selected from the RANGE to be used as the clock input to the accumulator. This selected frequency is counted for the duration of the gate pulse. The duration of the gate pulse in time interval measurements is determined by the specific slope and trigger level conditions set on channels A and B in relation to the signals present on the respective channels. Channel A sets the conditions for the start of the gate pulse, channel B for the end of the gate pulse. The same signal may be used on both channels, or separate signals may be used on each channel.

3-7. During ratio and totalize functions (RATIO A/B and A GTD. BY B), clock pulses from channel A are counted while the accumulator is gated by channel B. The number of pulses counted is displayed in the readout with no measurement units. When the ratio function is selected, the cycles of the channel A frequency are counted for a gate interval determined by a pre-selected number of cycles of the channel B frequency (the number of cycles is selected from the RANGE). The number, n, thus displayed, with decimal point automatically placed, is implied to be the ratio n:1. When the totalize function is selected, the number displayed represents the total number of triggering events that occurred at channel A during an operator-controlled or an externally programmed period of time. For this function, the gate pulse is a dc level obtained directly from channel B, rather than being a pulse derived from an input frequency as in the ratio function. Automatic recycling (resetting) is inhibited in the totalize function, and successive gate pulses cause the accumulator to resume counting without resetting to zero first. However, pressing the RESET button, or applying an external reset signal will manually reset the accumulator to zero.

3-8. The self-check function is used to test the 1953A for correct operation of the counting, gating and display circuits. In this function the display shows the total number of cycles of the 10 MHz reference frequency counted during a pre-selected gate time. The number

displayed has no units annunciated, and the gate time used is any of the six available in the RANGE, as in the frequency measurement functions. The digit-check subfunction is used to test the display LED's. When a reset signal (either manual or external) is applied in the self-check mode, all of the segment drivers are enabled and all correctly operating segments illuminate.

3-9. BLOCK DIAGRAM ANALYSIS

3-10. Channel A Amplifier

3-11. The function of the channel A input amplifier is to condition the input signal (type of coupling and attenuation), amplify it, and shape the signal before it is applied to the accumulator clock selector in the function control logic. As shown in Figure 3-2, the input signal to channel A can either be coupled across capacitor C402 (for AC coupling) or, by placing the front panel control to the DC position, applied directly to the attenuator. The attenuator switch can be placed to the X1 position to use the full amplitude of low level input signals or to the X10 position to reduce the input signal level by approximately ten.

3-12. The conditioned signal is then applied to one side of dual FET Q5. The voltage level applied to the other side of the FET is determined by the TRIGGER LEVEL control (R406). The push-pull amplifier (Q7 and Q8) provides U2 with an input that can be shaped by the amplifier and Schmitt trigger section. The output of U2 is then applied to the accumulator clock input selector and to the TRIG STAT driven section, Q11 through Q15. The drivers insure that for higher frequency inputs the TRIG STAT indicators on the front panel will light.

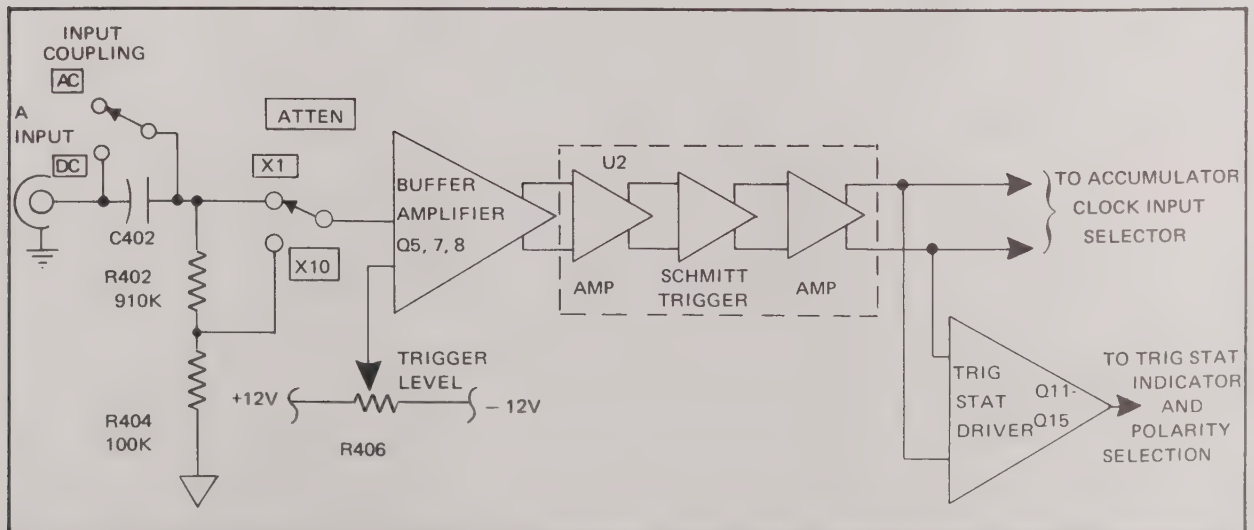


Figure 3-2. Channel A Input Amplifier

3-13. Channel B Amplifier

3-14. As shown in Figure 3-3, the signal conditioning for the input signals applied to channel B (input coupling and attenuation) is the same as that for channel A. The buffer amplifier (Q1, Q3 and Q4) also comprises a dual-FET, push-pull amplifier configuration the same as that in channel A, with the trigger level being determined by the TRIGGER LEVEL control (R405) for channel B. The difference between the two input channels is in the final stage of the channel B wave shaping circuit (U1, Q9, and Q10). The outputs of the Schmitt trigger portion of U1 are applied to the bases of Q9 and Q10 so that the output of the channel B amplifier is at a true TTL level.

3-15. Reference Generator

3-16. The 10 MHz basic signal for the reference oscillator (Figure 3-4) is provided either by the internal oscillator (U7) or through the EXT 10 MHz clock input jack on the rear panel of the instrument. The 10 MHz signal is applied to the gate of Q21, which is used to buffer the input of the amplifier (U21).

3-17. Function Control Logic

3-18. The function control logic receives signal data from the channel A, channel B and channel C input amplifiers and from the reference generator. From these inputs, the control logic, as directed by the range and function switch positions, selects the signal to be applied to the accumulator and controls the time interval for which it is applied. The operation of the function control logic will be discussed for each separate position of the function switch.

3-19. FUNCTION CONTROL LOGIC: FREQ. A

3-20. The basic signal processing that takes place in the control logic when the FREQ A function is selected is illustrated in Figure 3-5. The input selector (U4) will select either the leading or trailing edge (+ SLOPE, or - SLOPE) of the input A signal for triggering. The input A signal is then applied to one input of the main gate (U6).

3-21. The other input to U6 is the gate time signal. The gate time signal for the FREQ A function is derived from the 10 MHz reference generator signal. The 10 MHz signal is first applied to the reference fre-

quency divider (U11-U15) where it is reduced to a 10 kHz output. Reference divider input select gate U24 is directed by the FREQ A function command to apply the 10 kHz reference to the reference divider. The reference divider comprises a series of five decade counters that produce six separate frequency outputs; 10 kHz, 1 kHz, 100 Hz, 10 Hz, 1 Hz, and 0.1 Hz. The range selector (U26, U27 and U28) output frequency is controlled by the particular range selected. The gate selector (U42), also controlled by the FREQ A function command, applies the range selector output to the main gate. The main gate is enabled for one cycle of the gate time signal. The cycles of the input A frequency that occur during this single cycle of the gate time frequency are accumulated.

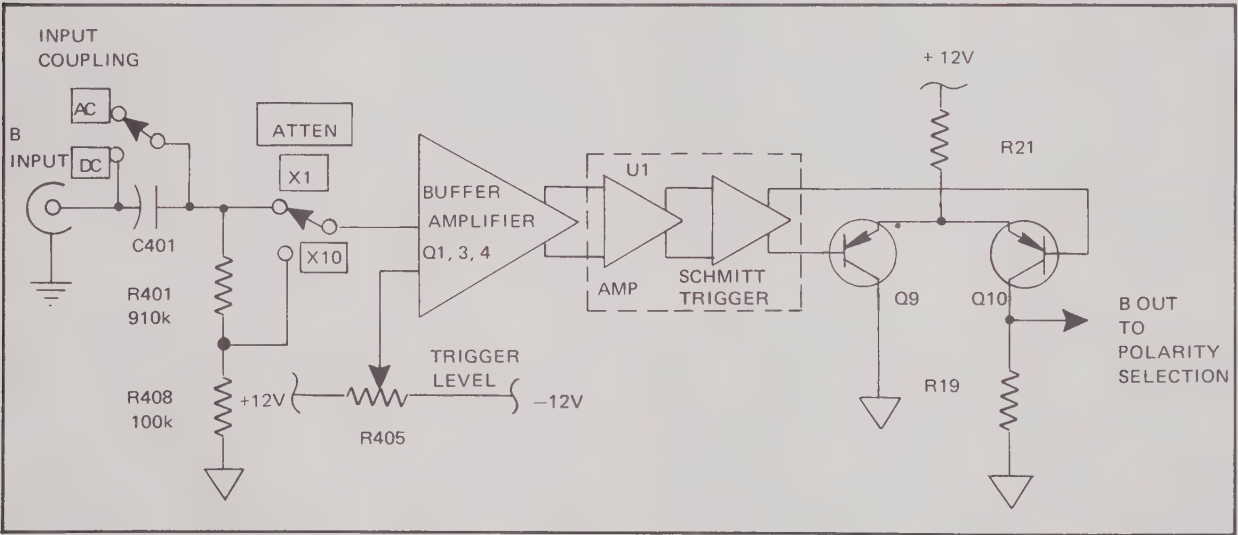


Figure 3-3. Channel B Input Amplifier

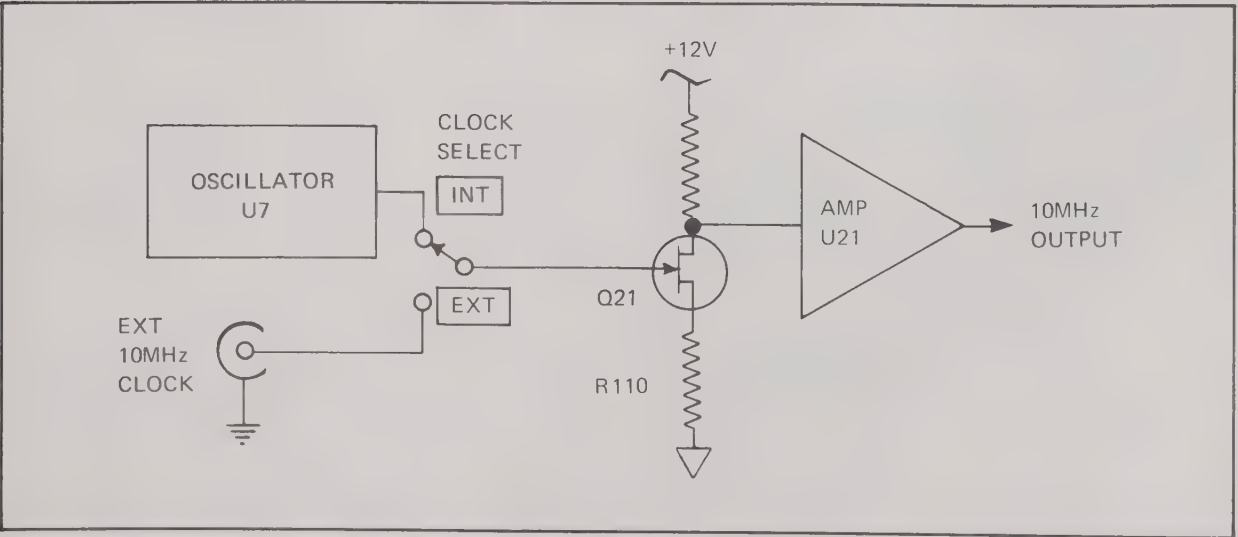


Figure 3-4. Reference Generator

3-22. FUNCTION CONTROL LOGIC: FREQ C

3-23. The operation of the function control logic for the FREQ C function (see Figure 3-6) is similar to that for the FREQ A function. The input select gate (U4) applies the signal output from the prescaler (Options -07, -13, and -14) to the main gate input as directed by the FREQ C function command.

3-24. The gate time for this function is again derived from the 10 MHz reference generator. The reference frequency divider circuit, however, receives a command from the function switch that introduces an additional division factor. The 10 MHz reference frequency is divided by four (Option -07) or eight (Options -13 and -14) to compensate for a similar frequency division applied to the channel C input signal by the respective prescaler options. The reference divider input select gate (U24) directs this modified reference frequency to the reference divider circuit. The reference divider again provides six separate output frequencies, one for each

range switch setting. The range selector gate (U26, U27 and U28), as directed by the RANGE switch, selects the proper gate signal to be applied to U42. The gate selector (U42) then applies this signal to the main gate to enable it to pass the input C signal to the accumulator.

3-25. FUNCTION CONTROL LOGIC: FREQ. A/B

3-26. In this mode of operation the instrument will count the number of cycles of the input A signal that occur during a selected number of cycles of the input B signal. This configuration is illustrated in Figure 3-7.

3-27. The output of the Channel B input amplifier is selected by the reference divider input select gate, in the FREQ A/B function, to be used as the reference signal. The input B signal is applied to the reference divider where it is divided by powers of ten from 10^0 through 10^5 . The range selector will then select one of the six outputs of the reference divider, as determined by the range switch position,

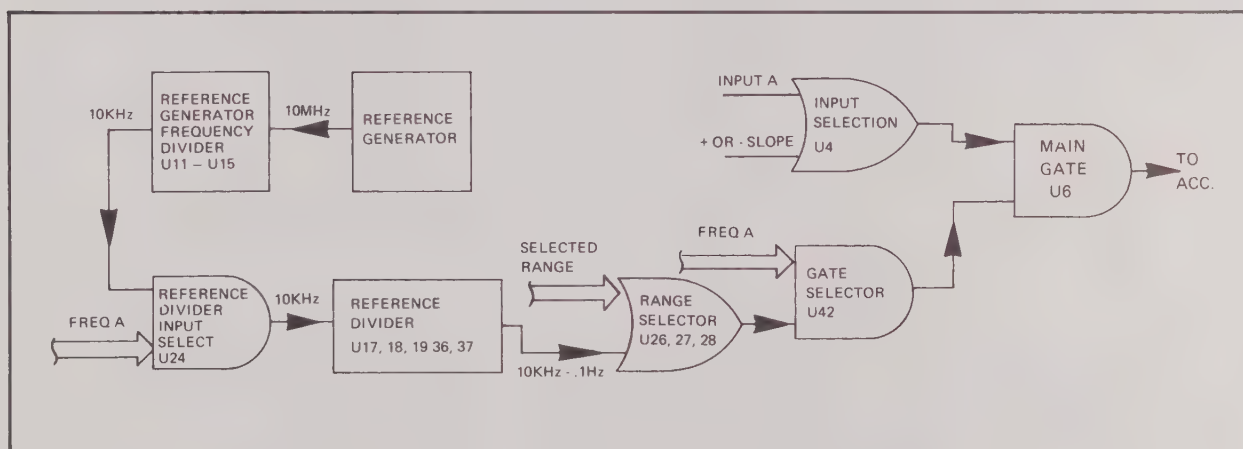


Figure 3-5. Function Control Logic: Freq. A

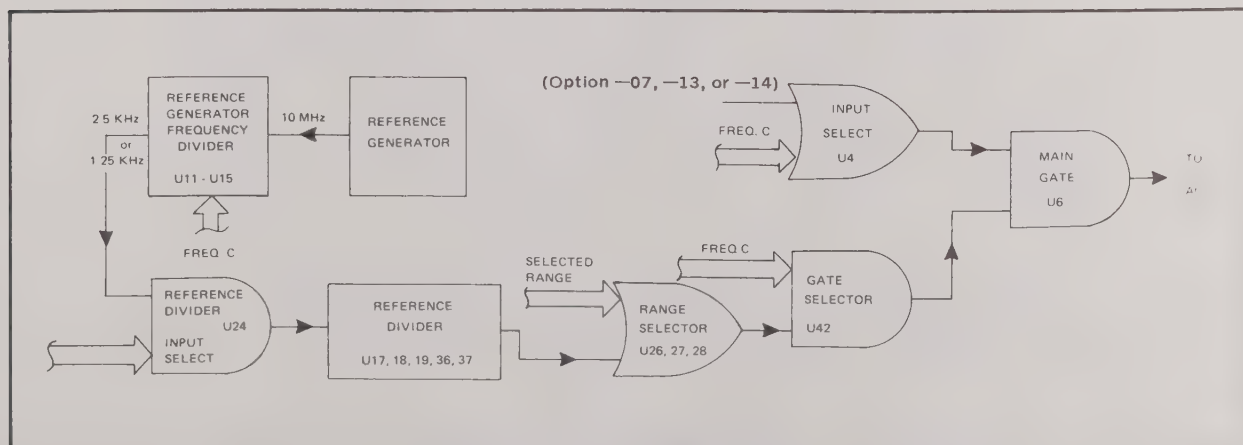


Figure 3-6. Function Control Logic: Freq. C

and apply it to the main gate to enable the gate to pass the input A signal to the accumulator.

3-28. FUNCTION CONTROL LOGIC: PERIOD A

3-29. The input signal applied to channel A is used as the reference frequency to enable the main gate while the 10 MHz reference generator signal is counted by the accumulator. Figure 3-8 illustrates this function control logic configuration.

3-30. The 10 MHz reference generator signal is directed, in the PERIOD A function, through the input selector (U23 and U41) to the main gate. The output frequency of the Channel A input amplifier is selected by the reference divider input select gate (U24) and applied to the reference divider. The six outputs of the reference divider consist, respectively, of the input A frequency divided by successive powers of 10 from 10^0 through 10^5 . The range selector applies the proper frequency, as determined by the range switch position, to the gate selector. The gate selector then enables the main gate for the duration of one cycle of the selected

frequency, during which time the 10 MHz reference generator signal is counted by the accumulator.

3-31. FUNCTION CONTROL LOGIC: T.I. A-B

3-32. In the T.I. A-B function the instrument uses the input signal on channel A to start the gate time pulse and the input signal on channel B to stop it. The time is measured by counting the number of cycles of the 10 MHz reference generator signal that occur during this period. Figure 3-9 shows the function control logic configuration for the T.I. A-B function.

3-33. The 10 MHz reference generator signal is directed through the reference divider input select (U24) to the reference divider. The six outputs of the dividers are: 10 MHz, 1MHz, 100 kHz, 10 kHz, 1kHz and 100 Hz. The range switch selects one frequency and applies it to the input selector which in turn applies it to the main gate. The gate time signal on the other input of the main gate is generated by the marker (U34, U43, U44) from the channel A and channel B inputs. The leading edge of the channel A input amplifier signal

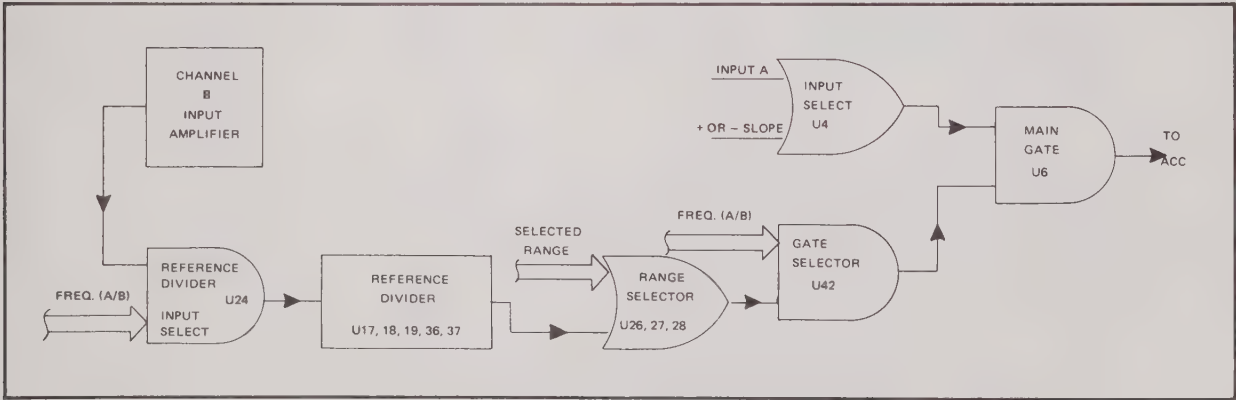


Figure 3-7. Function Control Logic: Freq. (A/B)

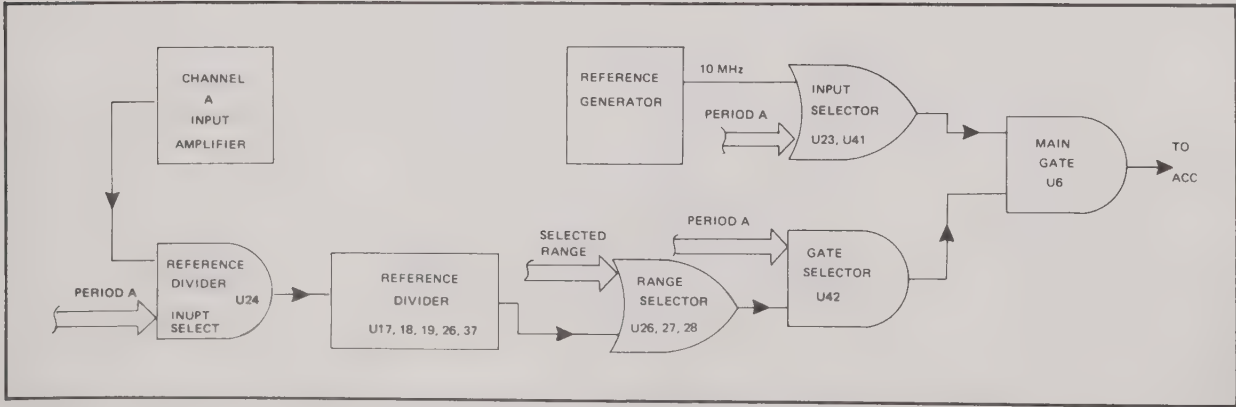


Figure 3-8. Function Control Logic: Period A

causes the output of the marker circuit to go low. This low signal causes the gate selector to enable the main gate. The leading edge of the channel B input amplifier signal causes the marker output to go high, which inhibits the main gate. The number of cycles of the reference frequency counted during this time is displayed as an amount of time in us or ms.

3-34. FUNCTION CONTROL LOGIC: A GTD. BY B

3-35. In the A GTD. BY B function the instrument will totalize the events that occur on the channel A input for a length of time determined by the channel B input. The function control logic for this mode of operation is illustrated in Figure 3-10.

3-36. The channel A input is directed through the input select gate (U4) to the main gate, in the A GTD. BY B function. The enable signal for the main gate comes from the channel B input amplifier through gate selector U42 and enables the main gate to pass the input A signal to the accumulator for counting.

3-37. FUNCTION CONTROL LOGIC: SELF CHECK

3-38. The Self Check function will check the control logic circuits for proper operation. Figure 3-11 shows the portions of the control logic used to perform the Self Check function.

3-39. Both the clock input to the main gate and the gate time are derived from the 10 MHz reference generator. The input selector (U4) directs the 10 MHz signal to one input of the main gate, in the Self Check function. The signal on the other input comes from the reference generator through the reference generator frequency divider to the reference divider input select gate. In the Self Check mode, a 10 kHz signal is directed to the reference divider. The Range selector directs one of the six reference divider output frequencies to the gate selector. The selected output frequency is applied to the main gate by the gate selector, and constitutes the main gate enable signal.

3-40. Accumulator

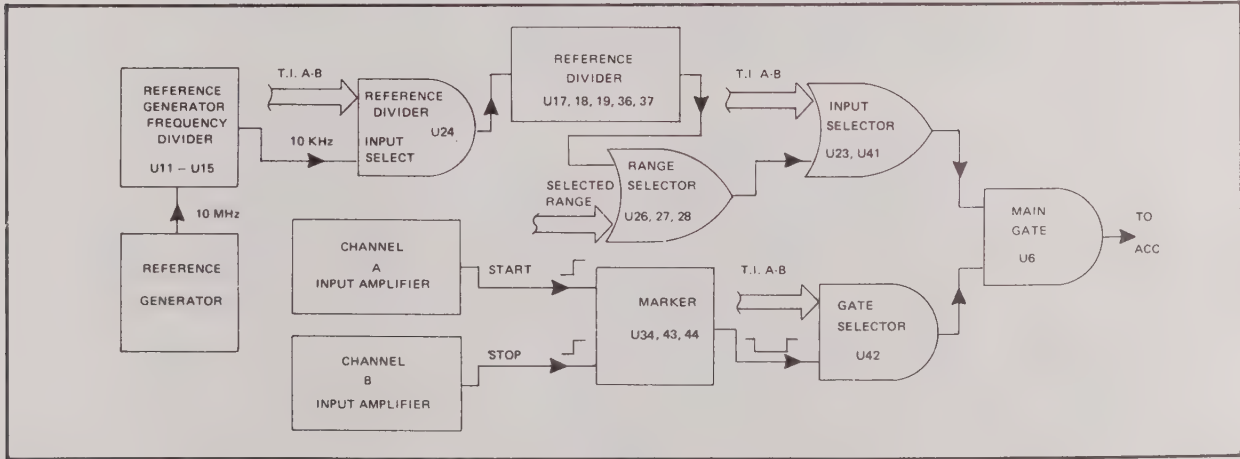


Figure 3-9. Function Control Logic: T.I. A-B

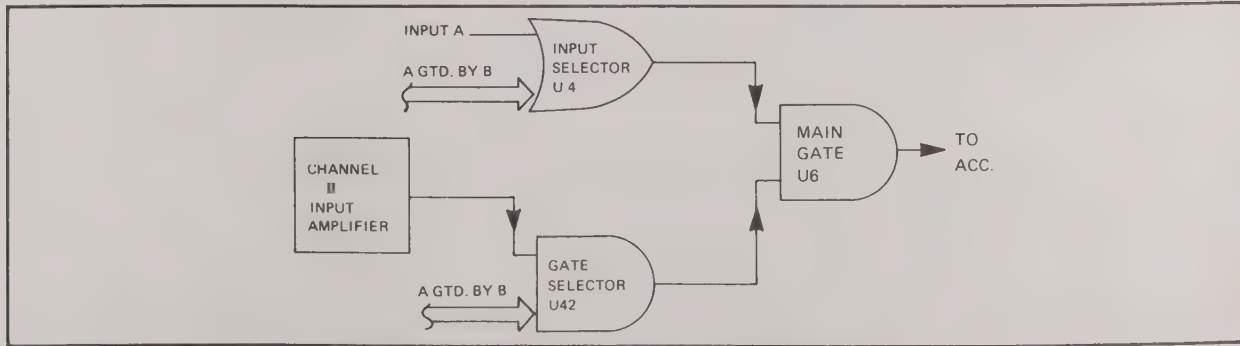


Figure 3-10. Function Control Logic: A GTD. BY B

3-41. The frequency of the accumulator input signal is equal to one-half the frequency of the signal applied to the main gate, U6. The gate is a J-K flip-flop with the input being applied to the clock terminal and the output taken from the Q terminal. The output of the main gate becomes the BCD A of the first digit. Figure 3-12 is a basic illustration of the accumulator.

3-42. Since the main gate is such an integral part of the first decade counter of the accumulator, it is represented in this block diagram as the CLK IN and J-K IN to the first decade counter. The first digit or LSD (Least Significant Digit) produces a BCD output (A-B-C-D signals) and applies it to the LSI chip, U65. The carry output from the LSD is connected to the clock input of the next decade counter, U57. This counter also produces a BCD output which is applied to U65. The carry output is applied to the LSI chip U65 which contains the remaining seven decade counters used to produce the nine digits of the display.

3-43. When the decade counters have counted the input signal frequency for the duration of the main gate enable signal, the BCD output of each decade counter is applied to a four-bit latch. The memory update command that enables the latches to receive the BCD input is triggered by the trailing edge of the main gate enable signal.

3-44. The BCD digit information is moved from the latches to the display one digit at a time. An oscillator and a ten stage ring counter within U65 produce sequential enable signals for the four-bit gates and their corresponding digit drivers. The BCD digit information is gated out of the four-bit gates to the BCD-to-seven segment decoder. The seven segment digit information for each significant digit is strobed by the digit driver signal so that it is displayed on the corresponding digit position of the display.

3-45. The zero suppression logic within the LSI chip will blank zeros to the left of the most significant digit displayed. If the most significant digit is to the right of the decimal point, suppression will occur to the left of the decimal point only. If the frequency of the signal applied to the accumulator clock input is high enough and the gate enable signal long enough the most significant digit (MSD) will produce a carry signal that will light the overflow indicator on the front panel. A reset command from the display logic circuits will return the decade counter to zero for each new measurement cycle.

3-46. Display Logic

3-47. The display logic performs three basic functions. First, it illuminates the proper annunciator (MHz, kHz, us, ms or s) as needed for each function and range setting. Secondly, it enables the correct decimal point, as directed by the range and function controls. Finally, it will update the display and reset the counters as directed by the gate enable signal and cycle rate control.

3-48. The annunciator control is illustrated in Figure 3-13 in a simplified form. In the frequency A or Frequency C function the MHz annunciator will light when the range switch is positioned to ranges 1, 2 or 3 (0.1 ms, 1.0 ms or 10 ms). When the range switch is positioned to ranges 5, 6 or 7 (0.1s, 1.0, or 10s) the output of U63 changes from a high to a low logic level. The low output, representing ranges 4, 5 or 6, is inverted and applied to one AND gate section of U62 to light the kHz annunciator. The T.I. A-B function will cause the ms annunciator to light in ranges 1, 2 and 3 and the us annunciator to light in ranges 4, 5 or 6. The PERIOD A mode in ranges 1, 2 or 3 causes the ms annunciator to light and in the 4, 5 or 6 range the s annunciator will light.

3-49. The decimal point logic enables one input of one of six AND gates so that the correct decimal point will

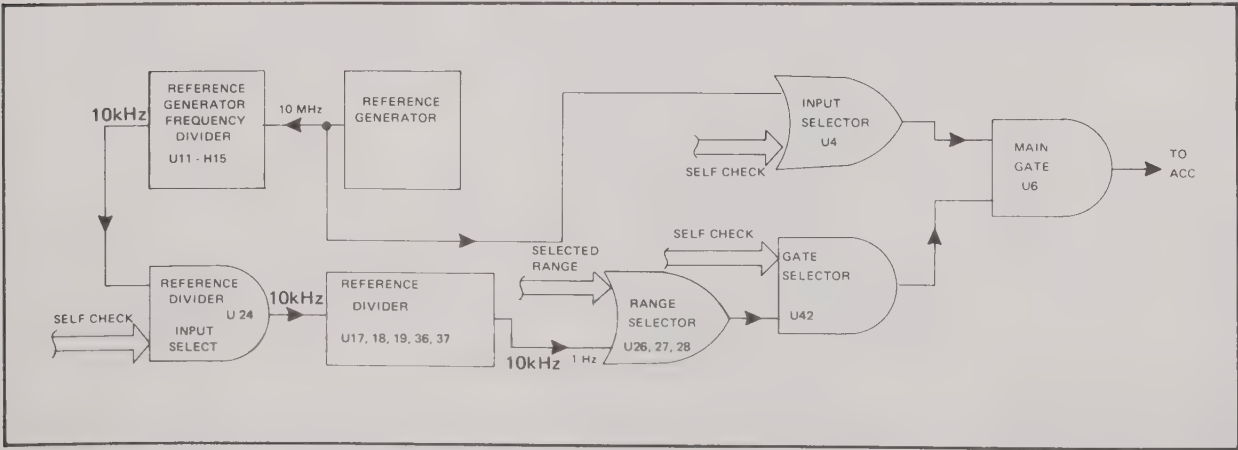


Figure 3-11. Function Control Logic: Self Check

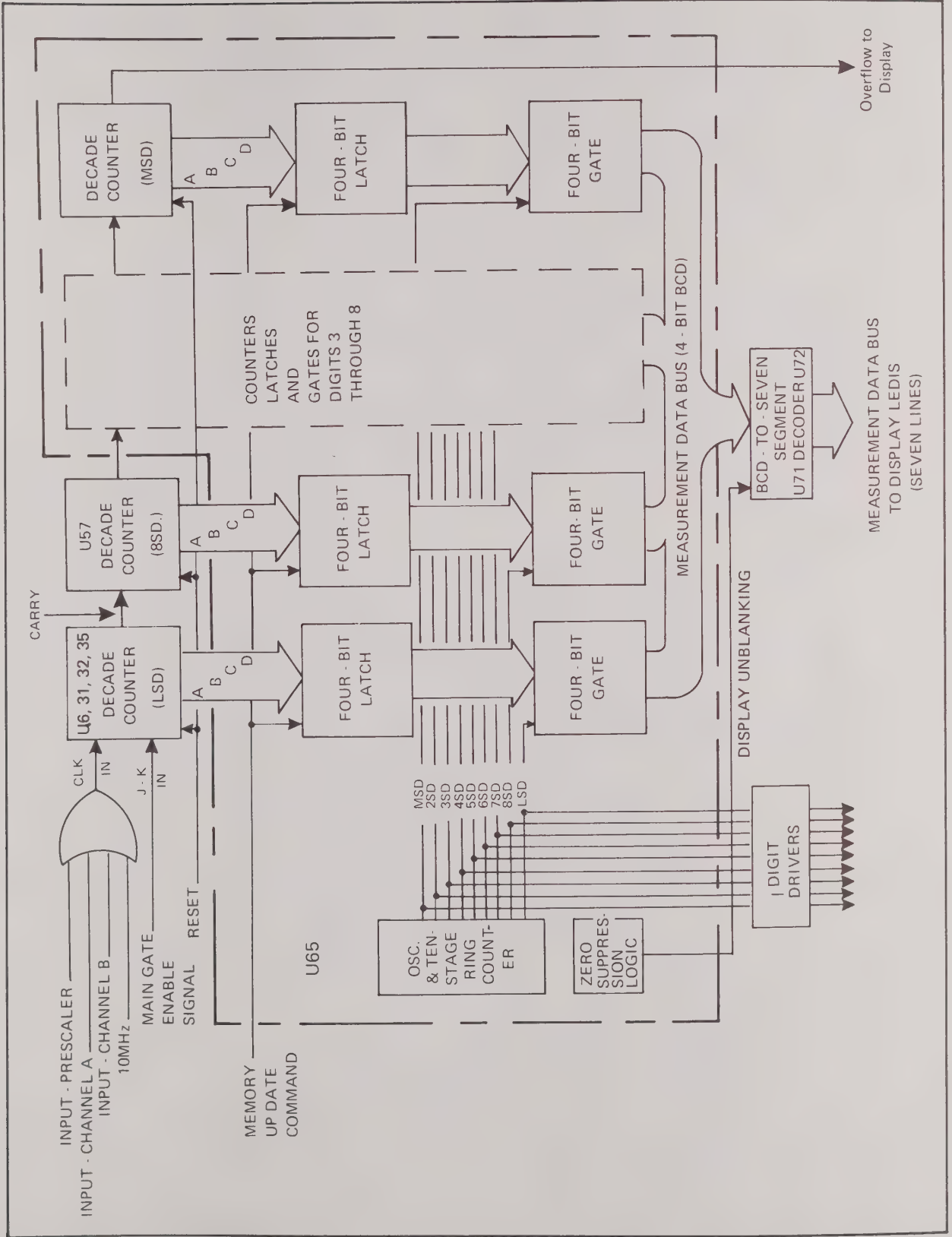


Figure 3-12. Accumulator, Block Diagram

light when a strobe signal is applied to the other input of the gate (see Figure 3-14). The range inputs are paired by NOR gates U52 and U53 (1 and 4, 2 and 5, 3 and 6) so that the decimal point will return to the same digit when either range is selected. This is used in the FREQ A, FREQ C, and T.I. A-B Functions because the annunciator changes the scale of the display between ranges 3 and 4. The function command input is combined with individual range commands, in order to place the decimal point at the proper digit.

3-50. The update and reset control provides commands, at the proper time, to update the digit information being displayed and to reset the decade counters for a new input (see Figure 3-15). At the end of the main gate enable pulse, U59 is set which enables U67 and the 100 kHz signal input to U66. The reaction time of U67 is controlled by the cycle rate control on the front panel, which delays the set command from U59 by 0.2 to 2 seconds. While the cycle rate delay is taking place the

100 kHz signal is clocking U66 through its outputs. The first cycle of the 100 kHz signal is used as a spacer between commands. The second cycle, however, causes U66 to output an update command. The third is again a spacer and the fourth causes the reset command output. The fifth cycle in will disable the 100 kHz input signal to stop the action in U66. At the end of the cycle rate delay, U67 will reset U59 which in turn resets U66, preparing the circuit for a new measurement cycle.

3-51. Display

3-52. The display consists of nine, seven-segment LED's. Figure 3-16 illustrates how the seven segment digit information and the decimal point information is applied to all nine display chips at the same time. The strobe lines, one to each display LED, enable the display digit that corresponds to the decade counter digit of the accumulator producing the digit information at that strobe time.

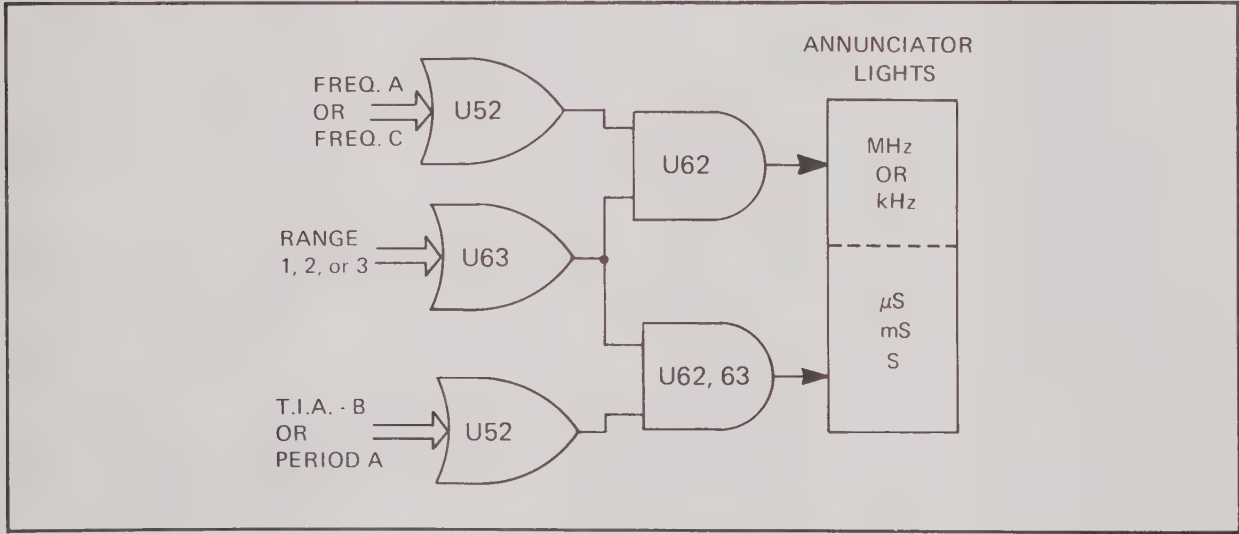


Figure 3-13. Annunciator Control Logic

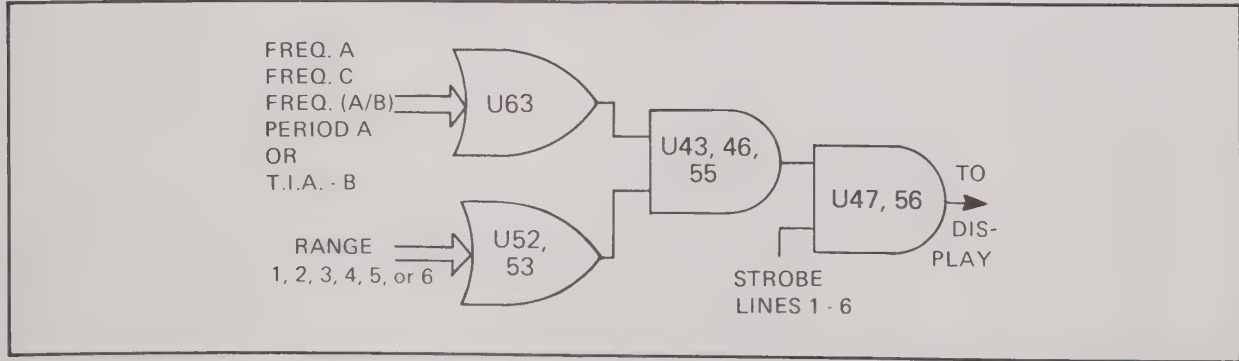


Figure 3-14. Decimal Point Control Logic

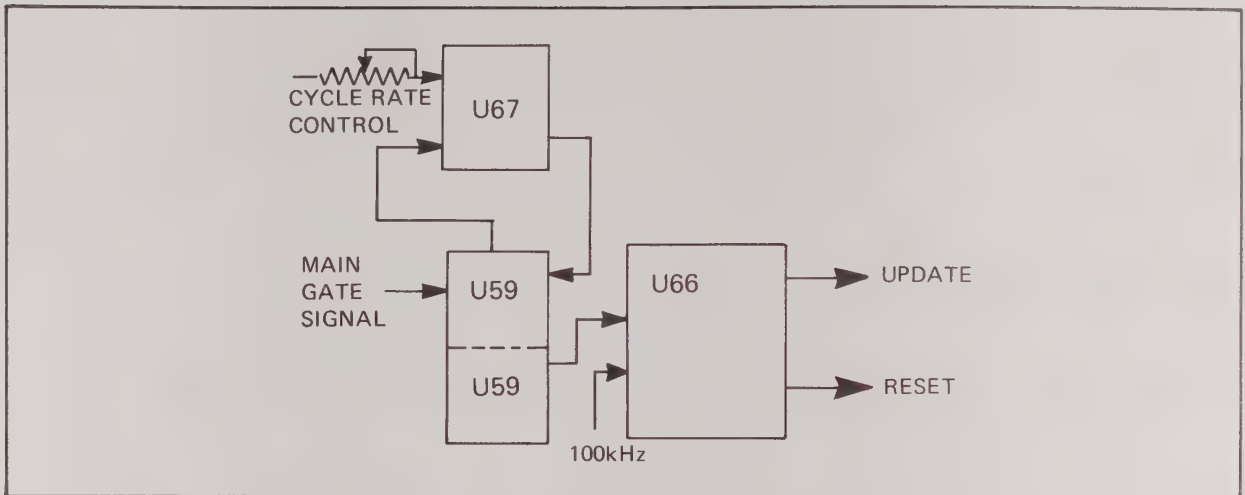


Figure 3-15. Update and Reset Control Logic

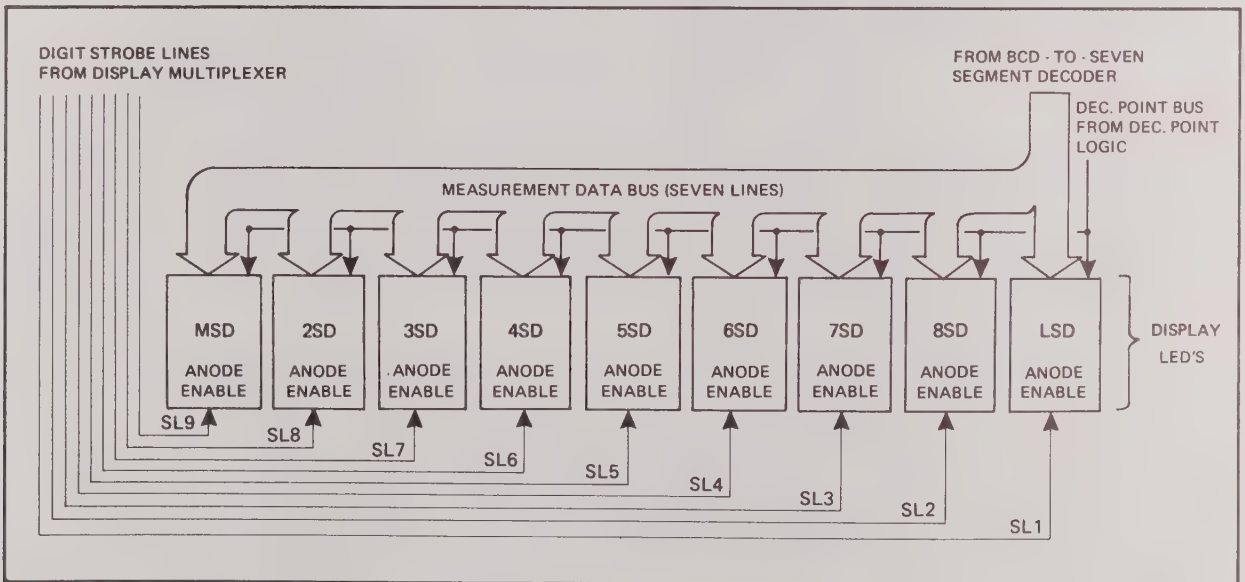


Figure 3-16. Display Section, Block Diagram

Section 4

Maintenance

4-1. INTRODUCTION

4-2. This section contains maintenance information for the Model 1953A Counter/Timer. This includes service information, general maintenance, performance test, calibration and troubleshooting. The performance test is recommended as a preventive maintenance tool and should be executed every 90 days to verify proper instrument operation. Troubleshooting information is given in the form of flowcharts at the end of this section. Table 4-1 lists the recommended test equipment required for maintenance of the 1953A.

4-3. SERVICE INFORMATION

4-4. Each instrument that is manufactured by the John Fluke Mfg. Co. Ltd. is warranted for a period of one year upon delivery to the original purchaser. The warranty is given on the back of the title page located in the front of this manual.

4-5. Factory authorized calibration and service for each Fluke product is available at various world-wide locations. A complete list of these service centers is included in Section 7. Shipping information is given in the operating instruction section of this manual. If requested, an estimate will be provided to the customer before work is begun on instruments that are beyond the warranty period.

4-6. GENERAL MAINTENANCE

Table 4-1. Test Equipment Required For 1953A Maintenance

EQUIPMENT NOMENCLATURE	RECOMMENDED MODEL	WHERE USED
Quartz oscillator frequency standard with 10 MHz output		Time base oscillator adjustment
Low frequency oscillator	HP 204D	Performance check calibration
High frequency oscillator	HP8654A HP 612A (for 1 GHz and 1.25 GHz options)	Performance check calibration
RF millivoltmeter with 50 ohm termination	Boonton 91C	Performance check calibration
Multimeter	Fluke 8000A	Troubleshooting
Oscilloscope	Tektronix 465	Troubleshooting

4-7. Access and Removal Information

4-8. All pcb assemblies used in the 1953A can be accessed for maintenance purposes by removing the top and the bottom dust covers from the instrument. Six Phillips - head screws hold each dust cover in place. Once both dust covers have been removed, the Front Panel assembly can be removed from the unit. Then the Display, the Switch, and the Input pcb assemblies can be removed from the Front Panel assembly. Use the procedures given in the following paragraphs to remove these pcb's from the unit. Repaired or replacement pcb's can be installed by reversing the procedures.

4-9. FRONT PANEL

4-10. Remove the Front Panel from the 1953A as follows:

- a. Remove top and bottom dust covers, by removing six Phillips screws from each cover.
- b. Unsolder input connector wires from input BNC jacks.
- c. Remove all front panel control knobs and the mounting nuts for the RESET button, and RANGE and FUNCTION switches.
- d. Remove single screw, holding Main pcb to Front Panel support bracket (front center, underside of Main pcb).
- e. Remove the two screws that hold the Display pcb and Input pcb to the front panel.
- f. Remove four screws holding Front Panel to side brackets (two on each side).

CAUTION!

During the next step, exercise care not to bend any of the pins that electrically interconnect the three pcb's to the Main pcb.

- g. Slide the front panel straight forward until it clears the switch shafts.

4-11. DISPLAY PCB ASSEMBLY

4-12. Remove the Display pcb assembly from the Front Panel assembly as follows:

- a. Complete procedure in Paragraph 4-9.
- b. Pull Display pcb away from front panel.
- c. Unplug the data input cable from J4 on the Main PCB.
- d. If power switch, CYCLE RATE Control or entire pcb is to be replaced, unsolder wires from power switch at rear of CYCLE RATE control.

4-13. SWITCH PCB ASSEMBLY

4-14. Remove the Switch pcb assembly from the Front Panel as follows:

- a. Complete procedure in Paragraph 4-9.
- b. Pull Switch pcb away from front panel.

4-15. INPUT PCB ASSEMBLY

4-16. Remove the Input pcb assembly from the Front Panel assembly as follows:

- a. Complete procedure in paragraph 4-9.
- b. Unsolder input connector leads.
- c. Pull Input pcb away from front panel.

4-17. Cleaning

4-18. Clean the 1953A periodically to remove dust, grease and other contamination. Use the following procedure:

- a. Clean the surface of all pcb's using clean, dry air at low pressure (≤ 20 PSI). If grease is encountered, spray with Freon T.F. Degreaser and remove grime with clean dry air at low pressure.
- b. Clean the front panel with a soft cloth dampened with a mild solution of detergent and water.

4-19. Fuse Replacement

4-20. The power fuse, F1, is located on the rear panel of the 1953A. If replacement is necessary, use a 1A slo-blo for 115V operation and a .5A slo-blo for 230V operation.

4-21. Service Tools

4-22. No special tools are required to maintain or repair the 1953A.

4-23. PERFORMANCE TEST

4-24. The performance test is designed to verify the overall operation of the 1953A. This test can be used as an acceptance check and/or periodic maintenance check. Table 4-1 lists the equipment required to perform this test. If the counter fails any part of the performance test, corrective action is indicated. Troubleshooting information for fault isolation is given later in this section.

4-25. Set-Up Procedure

4-26. Prior to executing the performance test, complete the following set-up procedure:

- a. Connect 1953A to line power.
- b. Rotate CYCLE RATE control cw, off the OFF detent and set to maximum cw position. The front panel display should light.

NOTE!

If the 1953A is equipped with the -10, -11, or -12 Option the rear panel MAIN POWER switch must be in the ON position.

- c. Set rear panel EXT/INT switch to INT.
- d. Set SEP/COM switch to SEP.
- e. Set CHANNEL A and CHANNEL B controls to following positions.
 1. TRIGGER LEVEL control to PRESET
 2. SLOPE switch to +.
 3. Coupling (AC/DC) switch to AC.
 4. ATTEN switch to X1

4-27. Channel A Amplifier Test

4-28. Use the following procedure to test the Channel A amplifier.

- a. Complete Set-Up Procedure.
- b. Connect a 2V rms, 1 kHz signal to CHANNEL A connector.
- c. Observe TRIG STAT annunciators. Both (+ and -) should be lit.
- d. Change settings of SLOPE, coupling and ATTEN switches. Both TRIG STAT annunciators should remain lit.
- e. Set the ATTEN switch to X10 and Coupling switch to AC.
- f. Turn TRIGGER LEVEL control cw, to just off PRESET DETENT' T PRESET detent. The + TRIG STAT annunciator should be lit, and the - annunciator off.
- g. Turn TRIGGER LEVEL control cw to center of its travel. Both TRIG STAT annunciators should be lit.

- h. Turn TRIGGER LEVEL control fully cw. The - TRIG STAT annunciator should be lit, and the + annunciator, off.

4-29. Channel B Amplifier Test

4-30. To test the channel B amplifier, repeat the procedure given in the previous paragraph, but use the CHANNEL B controls, indicators and connectors.

4-31. Display Test

4-32. Use the following procedure to test the front panel display:

- a. Complete Set-Up Procedure.
- b. Sequentially select each position of RANGE switch for each position of FUNCTION switch (except A GTD. by B). As each range is selected, verify that display is as described in Table 4-2. (A GTD. BY B position requires external inputs to test readout display.)
- c. Set FUNCTION switch to A GTD. BY B.
- d. Connect a 1V-rms, 5 Hz signal to CHANNEL A connector.
- e. Set CHANNEL A Coupling switch to DC.
- f. Set CHANNEL B SLOPE switch to —.
- g. Turn CHANNEL B TRIGGER LEVEL control cw until readout begins to display channel A input frequency. Observe least significant digit of readout and verify that each of 10 possible numerals (0 through 9) are displayed in sequence.
- h. Increase input frequency to 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz, pausing at each to verify proper operation of digits 2 through 7, respectively. (Digits are numbered from right to left).
- i. Use a 10 MHz signal to test digit 8 and a 100 MHz signal to test digit 9. Each digit will step through all ten numerals in ten seconds. Lower frequency signals will involve longer time intervals.
- j. Verify that OVERFLOW indicator lights as digit 9 steps from a 9 to a 0.
- k. Press RESET button (momentarily). Verify that OVERFLOW indicator goes out, readout resets to zero and totalizing process starts over.

Table 4-2. Display Readout With No Input Applied To Counter

FUNCTION SWITCH	RANGE SW	DISPLAY FOR AVAILABLE RANGE SETTINGS					
	INDICATIONS	1	2	3	4	5	6
DIGIT CHECK (SELF CHECK with RESET depressed)	READOUT	88888888	{same}	{same}	{same}	{same}	{same}
	ANNUNCIATOR	{none}	{none}	{none}	{none}	{none}	{none}
SELF CHECK	GATE t	0.1 ms	1.0 ms	10 ms	0.1 s	1.0 s	10 s
	READOUT	1000	10000	100000	1000000	10000000	100000000
	ANNUNCIATOR	{none}	{none}	{none}	{none}	{none}	{none}
T I. A-B	T I. RES.	0.1 ns	1.0 ns	10 ns	0.1 ns	1.0 ns	10 ns
	READOUT	0000	000	00	0000	.000	00
	ANNUNCIATOR	ms	ms	ms	s	s	s
PERIOD A	PER. AVGD	10 ⁰	10 ¹	10 ²	10 ³	10 ⁴	10 ⁵
	READOUT	.0000	.00000	.000000	.0000	.00000	.000000
	ANNUNCIATOR	ms	ms	ms	us	us	us
FREQ. (A/B)	PER. AVGD	10 ⁰	10 ¹	10 ²	10 ³	10 ⁴	10 ⁵
	READOUT	0	.0	.00	.000	.0000	.00000
	ANNUNCIATOR	{none}	{none}	{none}	{none}	{none}	{none}
FREQ. C	GATE t	0.1 ms	1.0 ms	10 ms	0.1 s	1.0 s	10 s
	READOUT	00	000	0000	00	000	0000
	ANNUNCIATOR	MHz	MHz	MHz	kHz	kHz	kHz
FREQ. A	GATE t	0.1 ms	1.0 ms	10 ms	0.1 s	1.0 s	10 s
	READOUT	00	.000	.0000	00	000	0000
	ANNUNCIATOR	MHz	MHz	MHz	kHz	kHz	kHz

4-33. Frequency A Test

4-34. Using the following procedure to test the frequency function:

- a. Complete Set-Up Procedure.
- b. Set FUNCTION switch to FREQ. A.
- c. Connect 1V rms, 100 kHz signal to CHANNEL A connector.
- d. Sequentially select each GATE t position of the RANGE switch, pausing at each to verify that the readout and measurement unit display are as described in Table 4-3.

4-35. Frequency C Test

4-36. The frequency C function is operational only when one of the Prescaler Options (-07, -13, or -14) has been installed.

Table 4-3. Display For Frequency A Test

GATE t	READOUT*	UNIT ANNUNCIATOR
0.1 ms	.10	MHz
1.0 ms	.100	MHz
10 ms	.1000	MHz
0.1 s	100.00	kHz
1.0 s	100.000	kHz
10 s	100.0000	kHz

*The accuracy of the readout is dependent on the accuracy of the 100 kHz input signal.

4-37. Ratio Test

4-38. Use the following procedure to test the ratio (frequency A/B) function:

- a. Complete Set-Up Procedure.
- b. Set FUNCTION switch to FREQ. A/B

- c. Set SEP/COM switch to COM.
- d. Connect 1V rms 100 kHz signal to CHANNEL A connector.
- e. Sequentially select each PER. AVGD. (periods averaged) position of RANGE switch, pausing at each to verify the readout display is as shown in Table 4-4. (No measurement unit annunciator will light).

Table 4-4. Display For Ratio Test

PER AVGD.	READOUT
10 ⁰	1
10 ¹	1.0
10 ²	1.00
10 ³	1.000
10 ⁴	1.0000
10 ⁵	1.00000

4-39. Period A Test

- 4-40. Use the following procedure to test the period A function:
- a. Complete Set-Up Procedure.
 - b. Set FUNCTION switch to FREQ A.
 - c. Connect 1V rms, 10 kHz signal to CHANNEL A connector.
 - d. Set RANGE switch to 10 s (GATE t) and adjust signal source to produce display of 10.000 kHz on readout.
 - e. Set FUNCTION switch to PERIOD A.
 - f. Sequentially select each PER. AVGD. position of RANGE switch, pausing at each to verify that display is as described in Table 4-5.

Table 4-5. Display For Period A Test

PER AVGD.	READOUT*	ANNUNCIATOR
10 ⁰	.1000	ms
10 ¹	.10000	ms
10 ²	.100000	ms
10 ³	100.0000	us
10 ⁴	100.00000	us
10 ⁵	100.000000	us

*The accuracy of the readout is dependent on the accuracy of the 10 kHz input signal.

4-41. Time Interval Test

- 4-42. Use the following procedure to test the time interval function:
- a. Complete Set-Up Procedure.
 - b. Set FUNCTION switch to FREQ. A.
 - c. Connect 1V rms, 5 Hz signal to CHANNEL A connector. (use a square wave with rise and fall times 15 ns).
 - d. Set RANGE switch to 10s (GATE t) and adjust signal source to produce display of .0050 on readout, (with kHz annunciator lit).
 - e. Set FUNCTION switch to T.I. A-B.
 - f. Set trigger level controls of channels A and B to PRESET. Set the CHANNEL A slope switch to + and the CHANNEL B slope switch to —.
 - g. Set SEP/COM switch to COM.
 - h. Sequentially select each T.I. RES. (time interval resolution) position of RANGE switch, pausing at each to verify that display is as described in Table 4-6.

Table 4-6. Display For Time Interval Test

T.I. RES	READOUT*	ANNUNCIATOR
0.1 us	100.0000	ms
1.0 us	100.000	ms
10 us	100.00	ms
0.1 ms	.1000	s
1.0 ms	.100	s
10 ms	.10	s

*The accuracy of the readout is dependent on the accuracy of the 5 Hz input signal.

4-43. Totalize Test

- 4-44. Use the following procedure to test the totalize (A gated by B) function:
- a. Complete Set-Up Procedure
 - b. Set FUNCTION switch to A GTD. BY B
 - c. Connect 1V rms, 100 Hz signal to CHANNEL A connector.

- d. Turn CHANNEL B TRIGGER LEVEL control cw until - TRIG STAT annunciator lights.
- e. Press and release RESET button. Readout should display 0 (zero). (Decimal point and measurement units are not displayed.)
- f. Turn CHANNEL B TRIGGER LEVEL control ccw until the + TRIG STAT annunciator lights. The 1953A should begin to count and display the total cycles of the 100 Hz input frequency. (Digit 3 should increment once per second.)
- g. Turn CHANNEL B TRIGGER LEVEL control ccw until TRIG STAT annunciator lights. The 1953A should stop counting and display accumulated total
- h. Repeat steps f and g. The accumulation process should take place as long as + TRIG STAT annunciator is lit. Notice that as steps f and g are repeated, displayed total is not reset. Instead, new inputs are added to previous total (totalized).

4-45. Self Check Test

- 4-46. Use the following procedure to test the self-check function:
- a. Complete Set-Up Procedure
 - b. Set FUNCTION switch to SELF CHECK
 - c. Depress the RESET switch. All display digit segments should illuminate. (No measurement unit annunciator will light.)
 - d. Sequentially select each GATE t position of the RANGE switch, pausing at each to verify display is as shown in Table 4-7. (No measurement unit annunciator will light).

Table 4-7. Display For Self-Check Test

GATE t	READOUT
0.1 ms	1000
1.0 ms	10000
10 ms	100000
0.1 s	1000000
1.0 s	10000000
10 s	100000000

4-47. CALIBRATION

- 4-48. The 1953A should be calibrated every 90 days or whenever repairs have been made. Calibration

should be done at an ambient room temperature of $25^{\circ} \pm 5^{\circ}\text{C}$. Table 4-1 lists the required test equipment.

4-49. +12 Volt Power Supply Adjustment

4-50. The +5 volt and -12 volt power supplies depend on the +12 volt supply for regulating and operating power. The adjustment of the +12 volt power supply will affect the other power supplies.

4-51. Calibrate the +12 volt supply as follows:

- a. Connect 1953A to ac line power.
- b. Connect positive input lead of DMM to +12V test point.
- c. Connect return lead of DMM to chassis ground.
- d. Set DMM to VDC on the 20 volt range.
- e. Turn CYCLE RATE control cw, off the OFF detent.
- f. Adjust the +12V adjustment (R97) for +12 $\pm 0.1\text{V}$.

4-52. Trigger Level Preset Adjustments.

4-53. This procedure outlines a check of the trigger level settings and, if required, an adjustment procedure. If desired the adjustment may be performed to achieve maximum sensitivity even though the trigger levels are within the listed specifications.

4-54. Check the Channel A preset trigger as follows:

- a. Perform or verify the following settings:
 1953A connected to ac line power
 POWER/CYCLE RATE fully clockwise
 CONT-TRIG switch to CONT
 RANGE to GATE t - 10 msec
 FUNCTION switch to FREQ A
 CHANNEL A controls—
 TRIGGER LEVEL to PRESET
 SLOPE to +
 AC-DC to AC
 ATTEN to X1
 CHANNEL B controls—
 TRIGGER LEVEL to PRESET
 SLOPE to +
 AC-DC to AC
 ATTEN to X1
 SEP-COM switch to SEP

- b. Connect the High Frequency Signal Generator and the RF Voltmeter Probe to the CHANNEL A input

connector through a 50Ω termination "T" connector.

- c. Set the High Frequency Signal Generator for an input to the 1953A of 75 MHz at 30V rms.
30 mV RMS
- d. The display is stable and reads the input frequency.
- e. Set the High Frequency Signal Generator for an input to the 1953A of 125 MHz at 50V rms.
50 mV RMS
- f. The display is stable and reads the input frequency.
- g. If either reading is unstable perform the adjustment procedure in the subparagraphs below. If acceptable, proceed to the next paragraph.
- h. Set the High Frequency Signal Generator for an input to the 1953A of 125 MHz at 45 mV rms.
- i. Set the Channel A internal trigger level trimpot, R34, fully counterclockwise. Rotate R34 slowly clockwise until the display is stable at the input frequency of 125 MHz. Note the position of the R34 setting.
- j. Continue rotating R34 clockwise until the display becomes unstable again. Note the position of the R34 setting.
- k. Set R34 at the midpoint between the two settings obtained in steps i and j.
- l. Set the CHANNEL A SLOPE switch to "." and verify the display remains stable. Return the SLOPE switch to the "+" position.
- m. Lower the amplitude of the Signal Generator until the display starts to become unstable.
- n. Repeat steps i through m until maximum sensitivity is achieved.

4-55. Check the Channel B preset trigger as follows:

- a. Perform or verify the following settings:
1953A connected to ac line power
POWER/CYCLE RATE fully clockwise
CONT-TRIG switch to CONT
Range to PER AVG D -10^3
FUNCTION switch to FREQ (A/B)
CHANNEL A controls—
TRIGGER LEVEL to PRESET
SLOPE to +
AC-DC to AC
ATTEN to X1
CHANNEL B controls—
TRIGGER LEVEL to PRESET
SLOPE to +

AC-DC to AC
ATTEN to X1
SEP-COM switch to COM

- b. Connect the High Frequency Signal Generator and the RF Voltmeter Probe to the CHANNEL A input connector through a 50Ω termination "T" connector.
- c. Set the High Frequency Signal Generator for an input to the 1953A of 25 MHz at 30 mVolts.
- d. The display is stable and reads the input frequency.
- e. If the reading is unstable perform the adjustment procedure in the subparagraphs below. If acceptable, proceed to the next paragraph.
- f. Set the High Frequency Signal Generator for an input to the 1953A of 25 MHz at 25 mVolts.
- g. Set the Channel B internal trigger level trimpot, R35 slowly clockwise until the display is stable at the input frequency of 25 MHz. Note the position of the R35 setting.
- h. Continue rotating R35 clockwise until the display becomes unstable again. Note the position of the R35 setting.
- i. Set R35 at the midpoint between the two settings obtained in steps g and h.
- j. Set the CHANNEL B SLOPE switch to "." and verify the display remains stable. Return the SLOPE switch to the "+" position.
- k. Lower the amplitude of the Signal Generator until the display starts to become unstable.
- l. Repeat steps g through k until maximum sensitivity is achieved.

4-56. Reference Generator Adjustment

4-57. Calibrate the 10 MHz temperature compensated crystal oscillator (TCXO) as follows:

- a. Connect 1953A to ac line power.
- b. Turn CYCLE RATE control cw, off the OFF detent.
- c. Set FUNCTION switch to FREQ. A.
- d. Set CONT/TRIG switch to TRIG.
- e. Connect 10 MHz frequency standard to CHANNEL A connector.

- f. Adjust CHANNEL A trigger level control to establish desired trigger condition. (Proper triggering occurs when + and - TRIG STAT annunciators are both lit.)
- g. Set RANGE switch to 1s (GATE t)
- h. Momentarily press RESET switch. After 1 second 1953A should light and display 10000.000 kHz.
- i. If display is incorrect, locate adjustment screw on TCXO (U7) on Main Board. (Bottom dust cover has hole to admit turning tool.) Using insulated tuning tool, adjust screw.
- j. Repeat steps h and i until proper display is obtained.

4-58. TROUBLESHOOTING

4-59. The following information is designed to aid in troubleshooting the 1953A. Fault area isolation is achieved by performing the operation steps as described in Section 2 and isolating the problem to a functional logic group using troubleshooting flowcharts. The flowchart symbols are defined in Figure 4-1 and the troubleshooting flowcharts are given in Figure 4-2. Figure 4-3 shows the locations of test points on the main PCB.

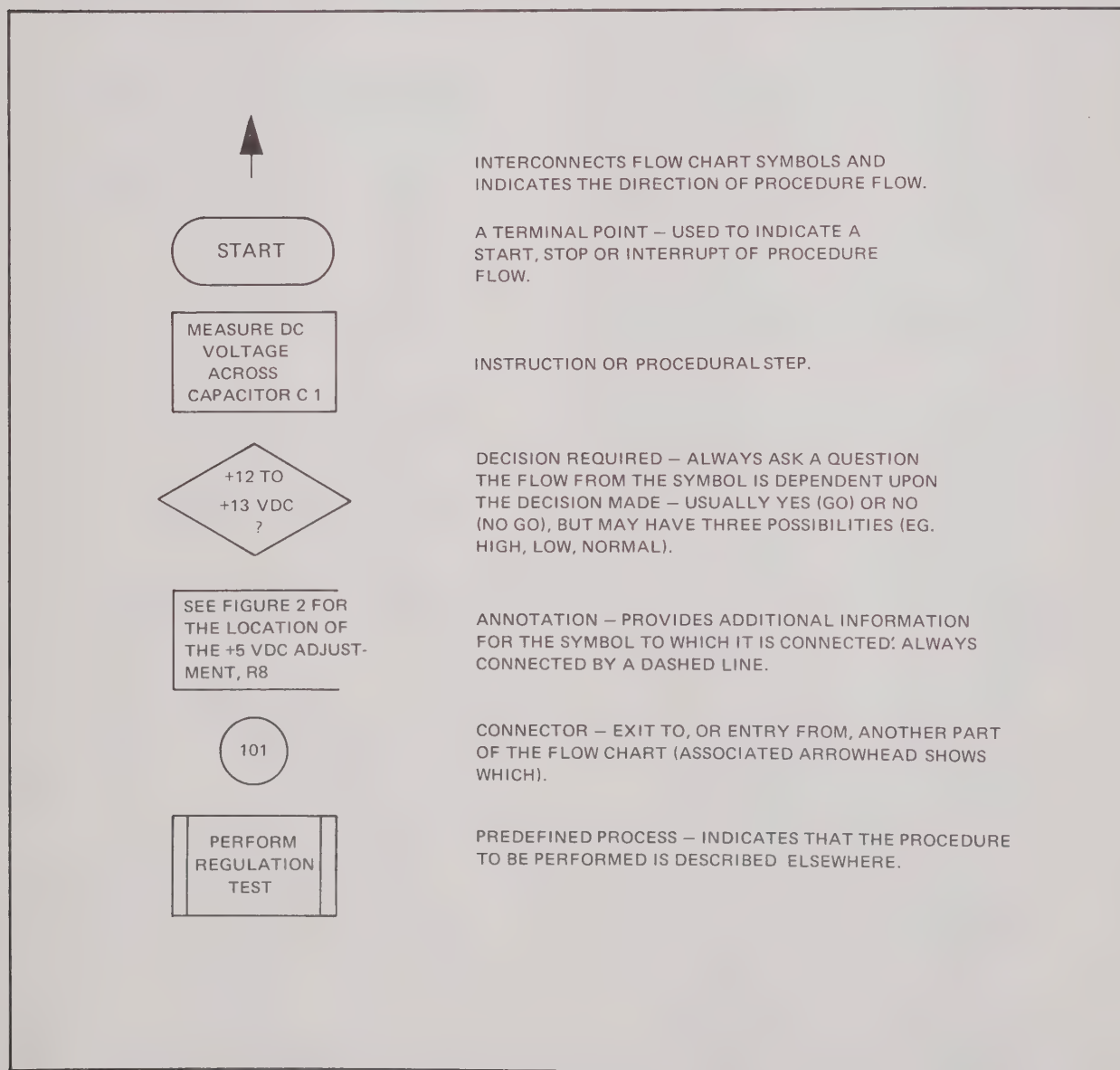


Figure 4-1. Troubleshooting Flowchart Symbols

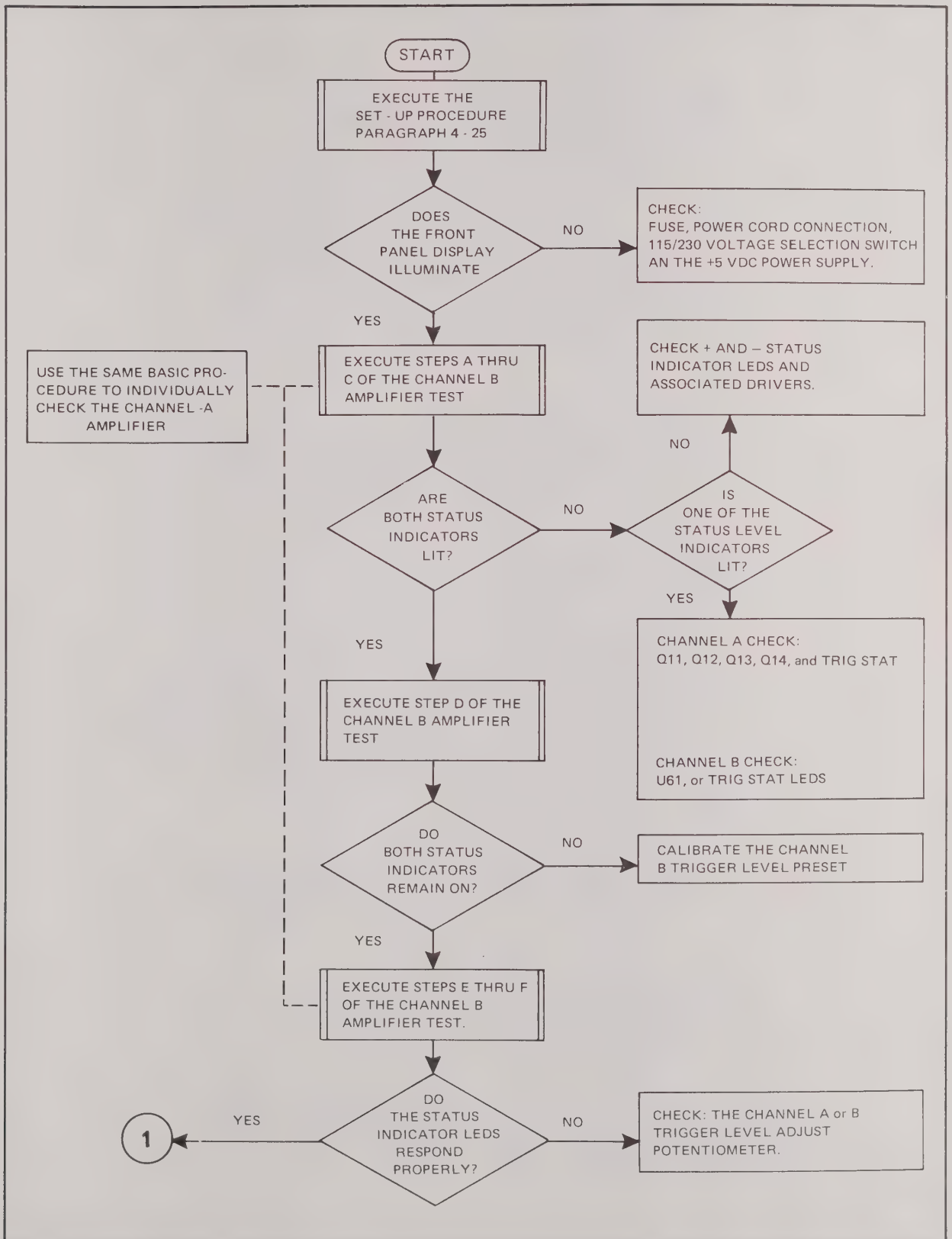


Figure 4-2. Troubleshooting Flowchart (Sheet 1 of 6)

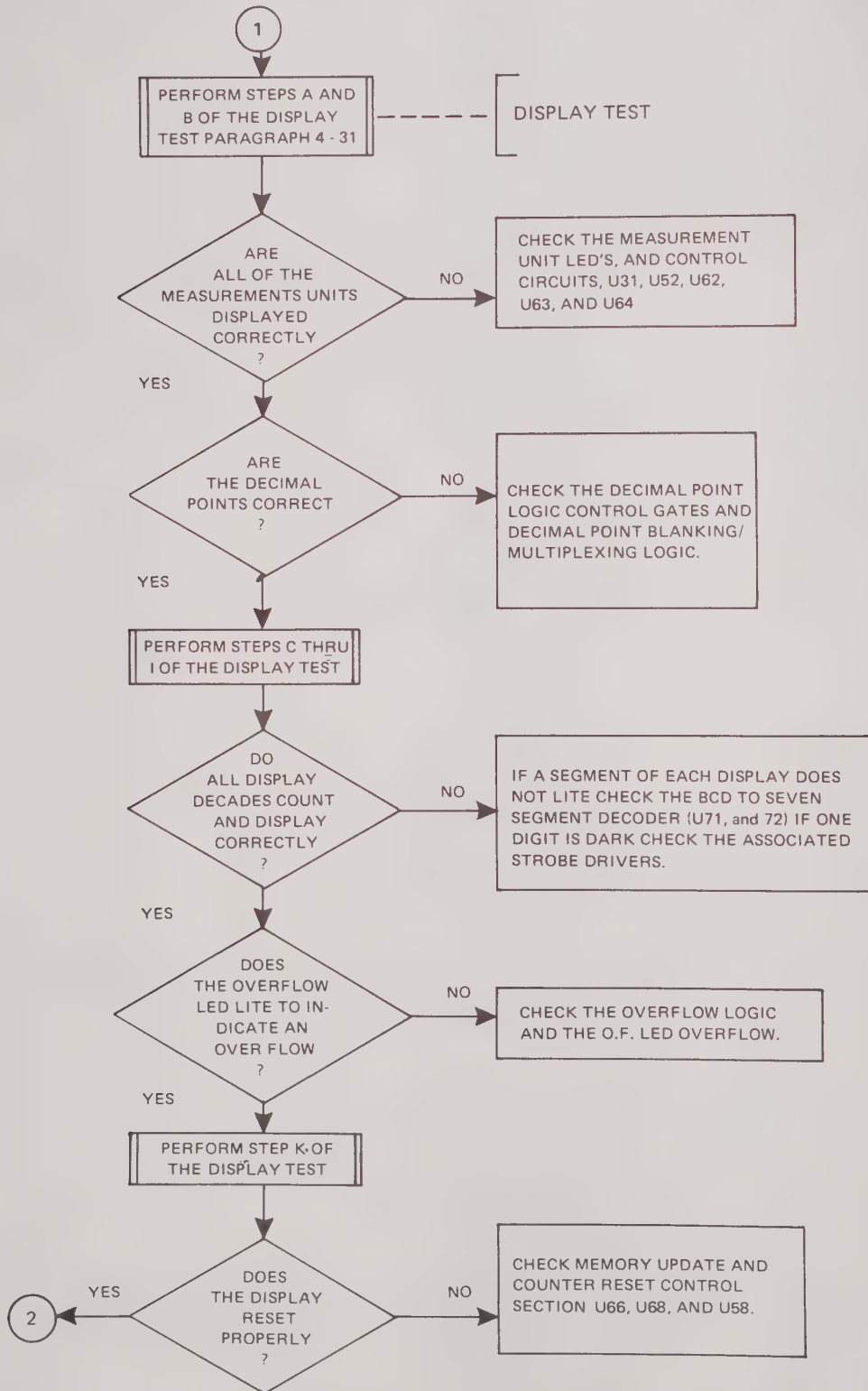


Figure 4-2. Troubleshooting Flowchart (Sheet 2 of 6)

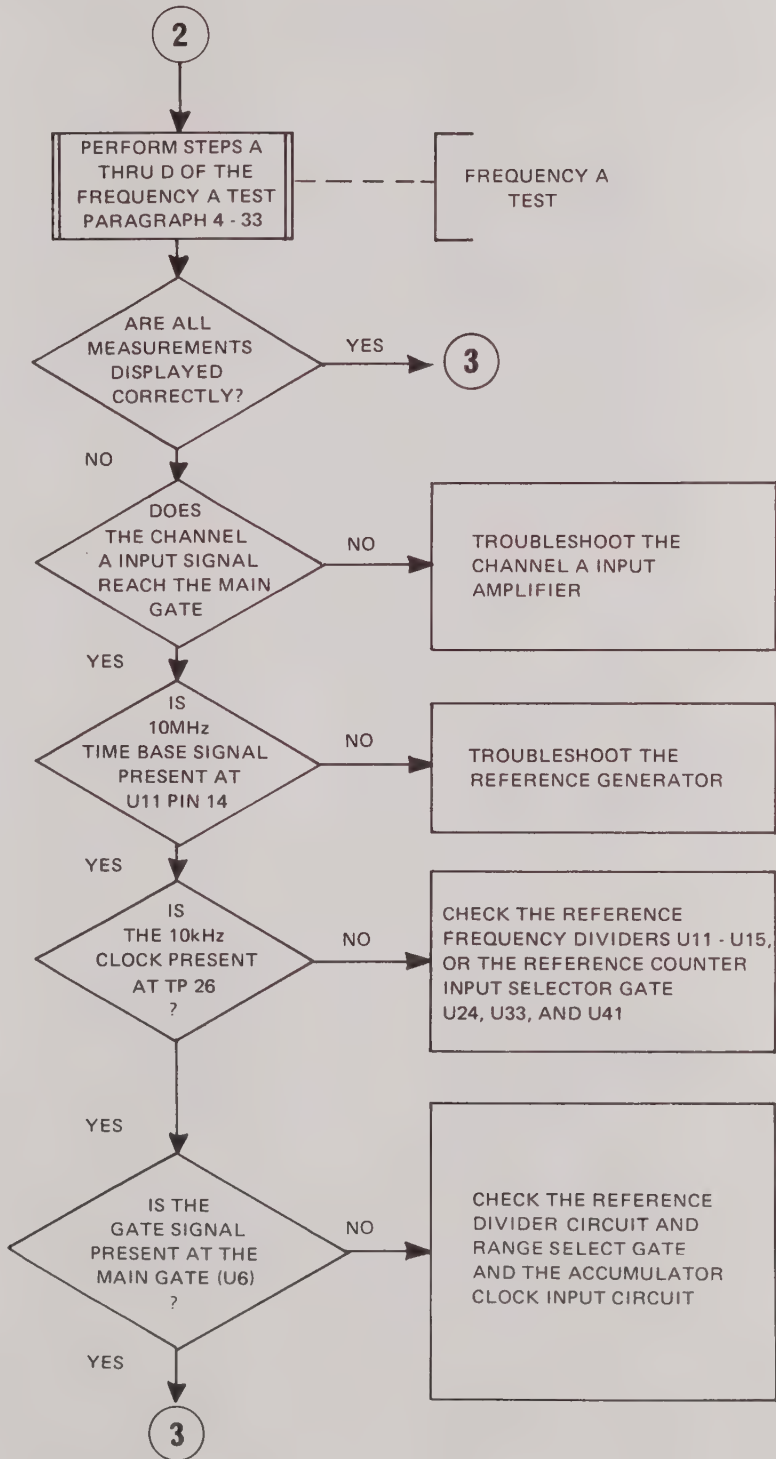


Figure 4-2. Troubleshooting Flowchart (Sheet 3 of 6)

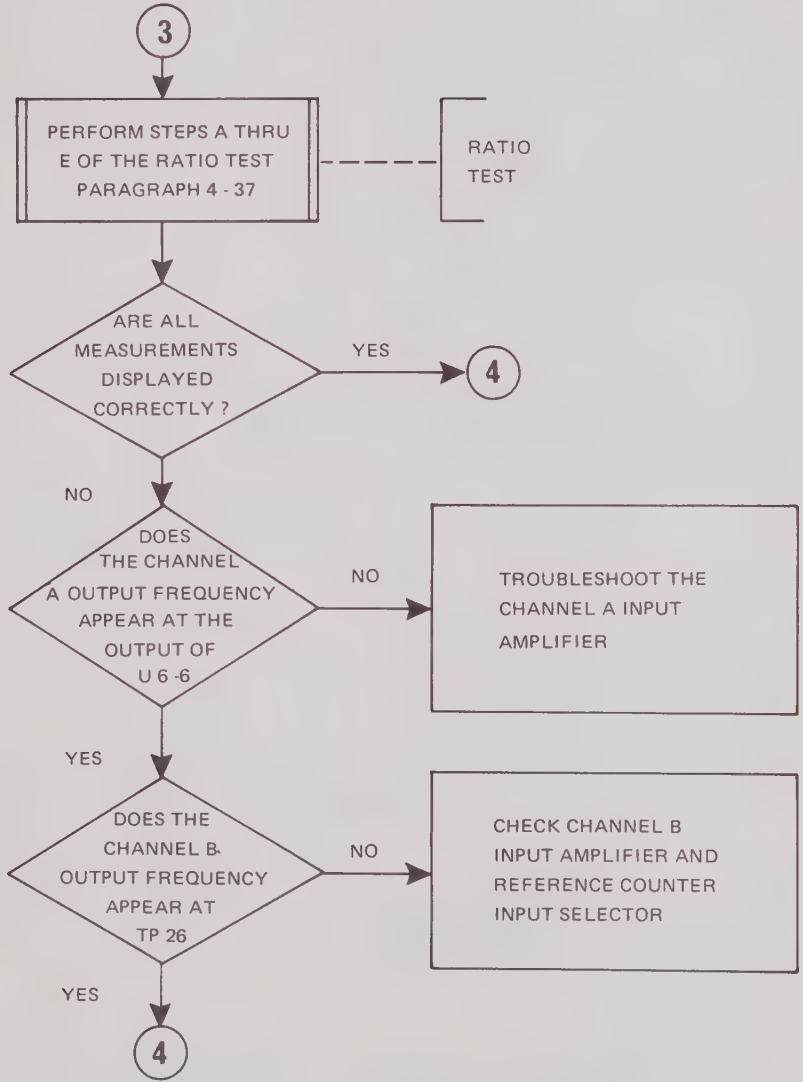


Figure 4-2. Troubleshooting Flowchart (Sheet 4 of 6)

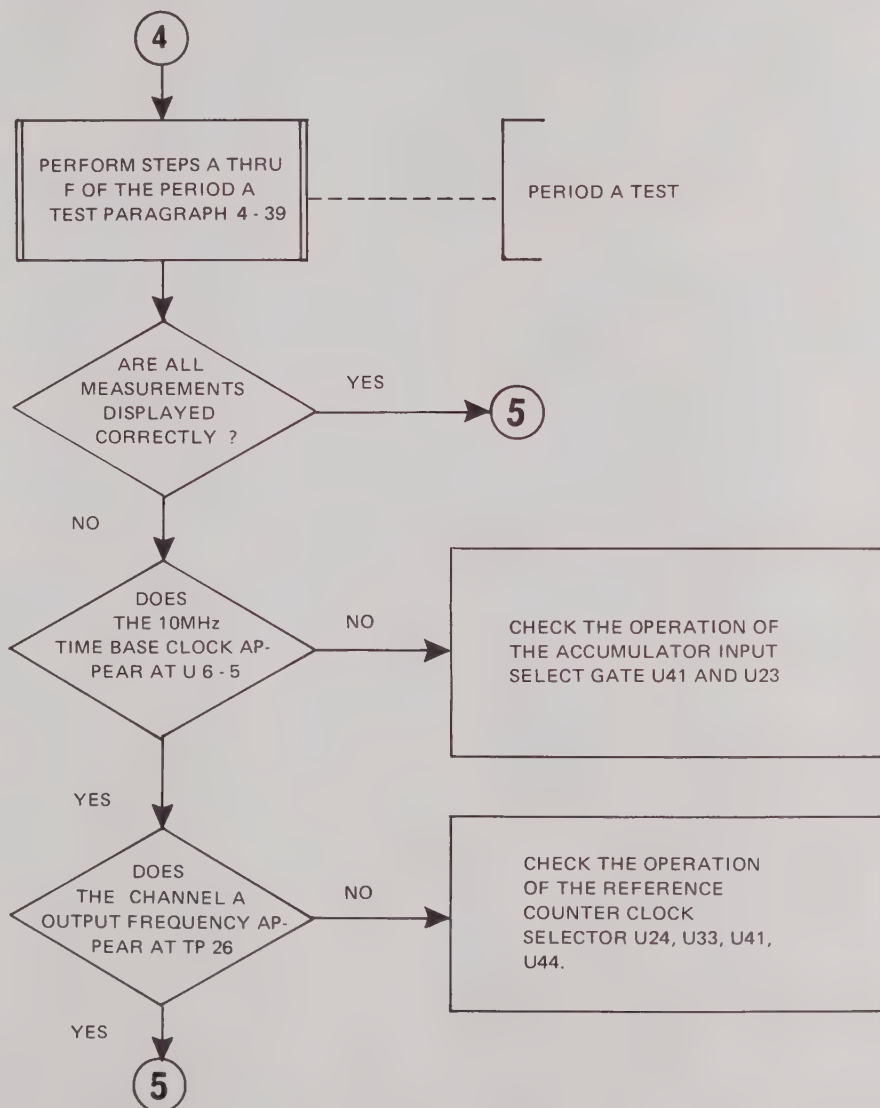


Figure 4-2. Troubleshooting Flowchart (Sheet 5 of 6)

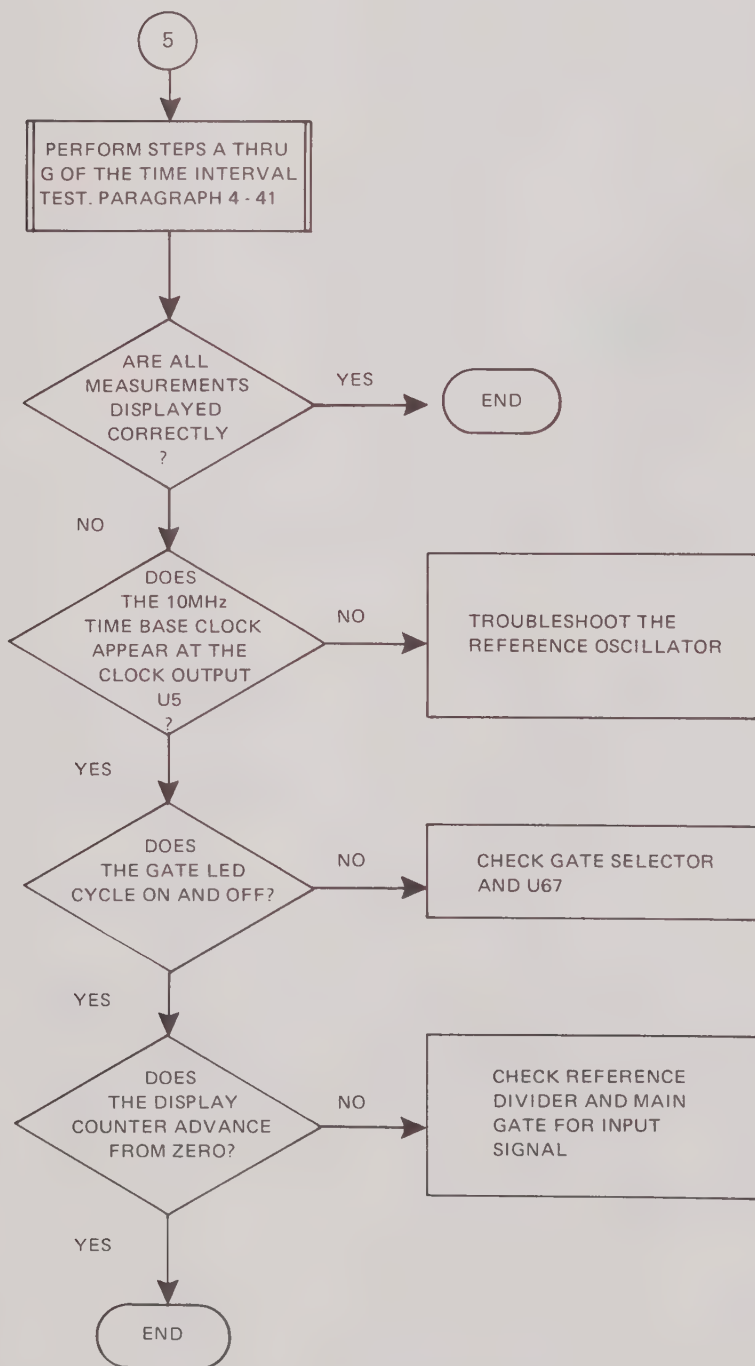


Figure 4-2. Troubleshooting Flowchart (Sheet 6 of 6)

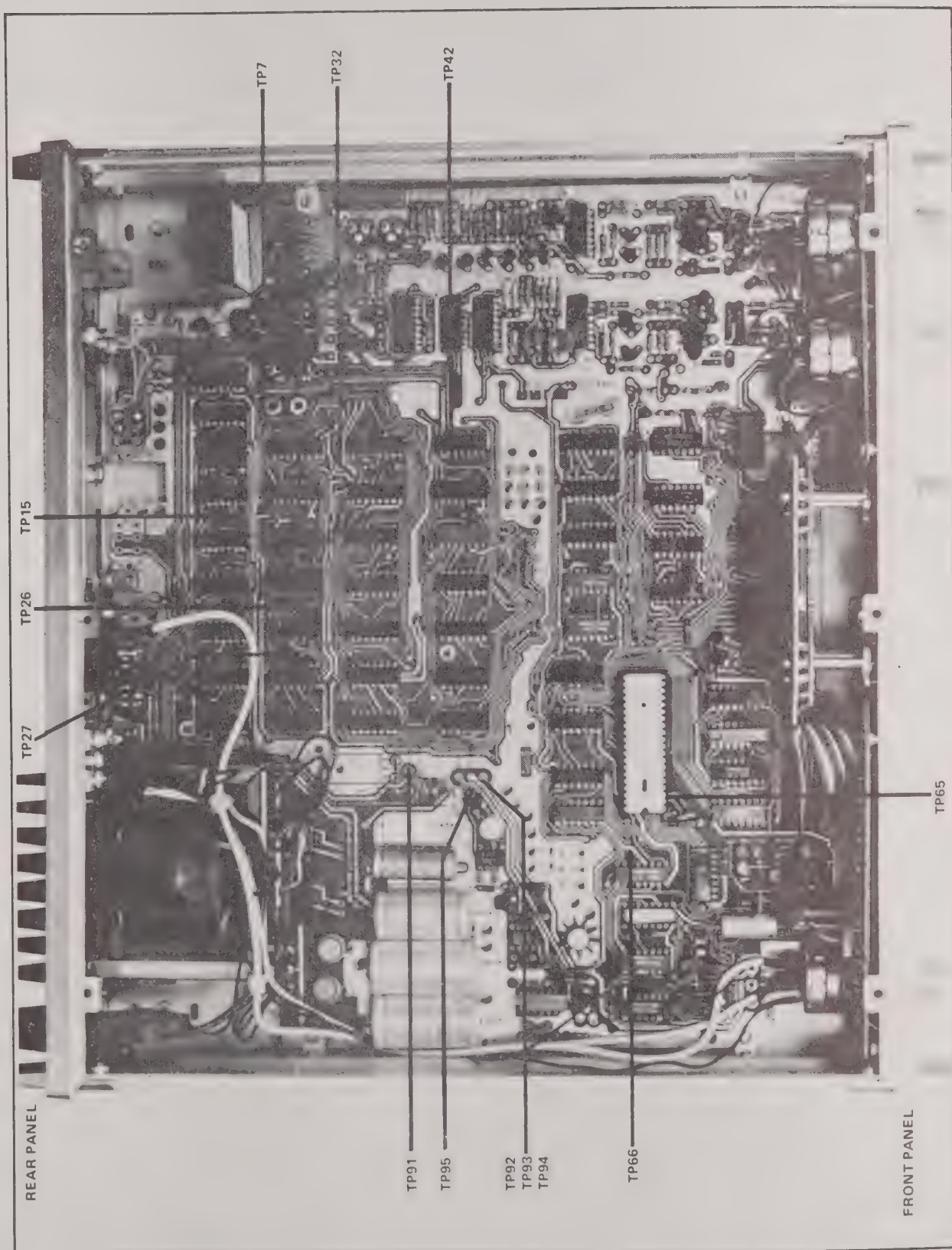


Figure 4-3. Test Point Locations, Main PCB

Section 5

List of Replaceable Parts

TABLE OF CONTENTS

TABLE	ASSEMBLY NAME	PART NO.	PAGE
5-1	Final Assembly, Model 1953A	398693	5-3
5-2	Main PCB Assembly	396200	5-10
5-3	Display PCB Assembly	396218	5-18
5-4	Switch PCB Assembly	396226	5-20
5-5	Input PCB Assembly	396234	5-22

5-1. INTRODUCTION

5-2. This section contains an illustrated parts breakdown of the instrument. Components are listed alphabetically by assembly. Electrical components are listed by reference designation and mechanical components are listed by item number. Each listed part is shown in an accompanying illustration.

5-3. Parts lists include the following information:

- a. Reference Designation or Item Number.
- b. Description of each part.
- c. Fluke Stock Number.
- d. Federal Supply Code for Manufacturers. (See Appendix A for Code-to-Name list.)
- e. Manufacturer's part Number or Type.
- f. Total Quantity per assembly or component.
- g. Recommended Quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of two years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for one year or more at an isolated site it is recommended that at least one in each assembly in the instrument be stocked. In the case of optional subassemblies, plug-ins, etc. that are not always part of the instrument, or are deviations from the basic instrument mode, the REC QTY column lists the recommended quantity of the item in that particular assembly.
- h. The Use Code is provided to identify certain parts that have been added, deleted or modified during

production of the instrument. Each part for which a use code has been assigned may be identified with a particular instrument serial number by consulting the Use Code Effectivity, paragraph 5-7.

5-4. HOW TO OBTAIN PARTS

5-5. Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co. Ltd. factory or authorized representative by using the **FLUKE STOCK NUMBER**. In the event the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

5-6. To ensure prompt and efficient handling of your order, include the following information:

- a. Quantity
- b. **FLUKE** Stock Number
- c. Description
- d. Reference Designation or Item Number
- e. Printed Circuit Board Part Number
- f. Instrument model and Serial number

5-7. USE CODE EFFECTIVITY LIST

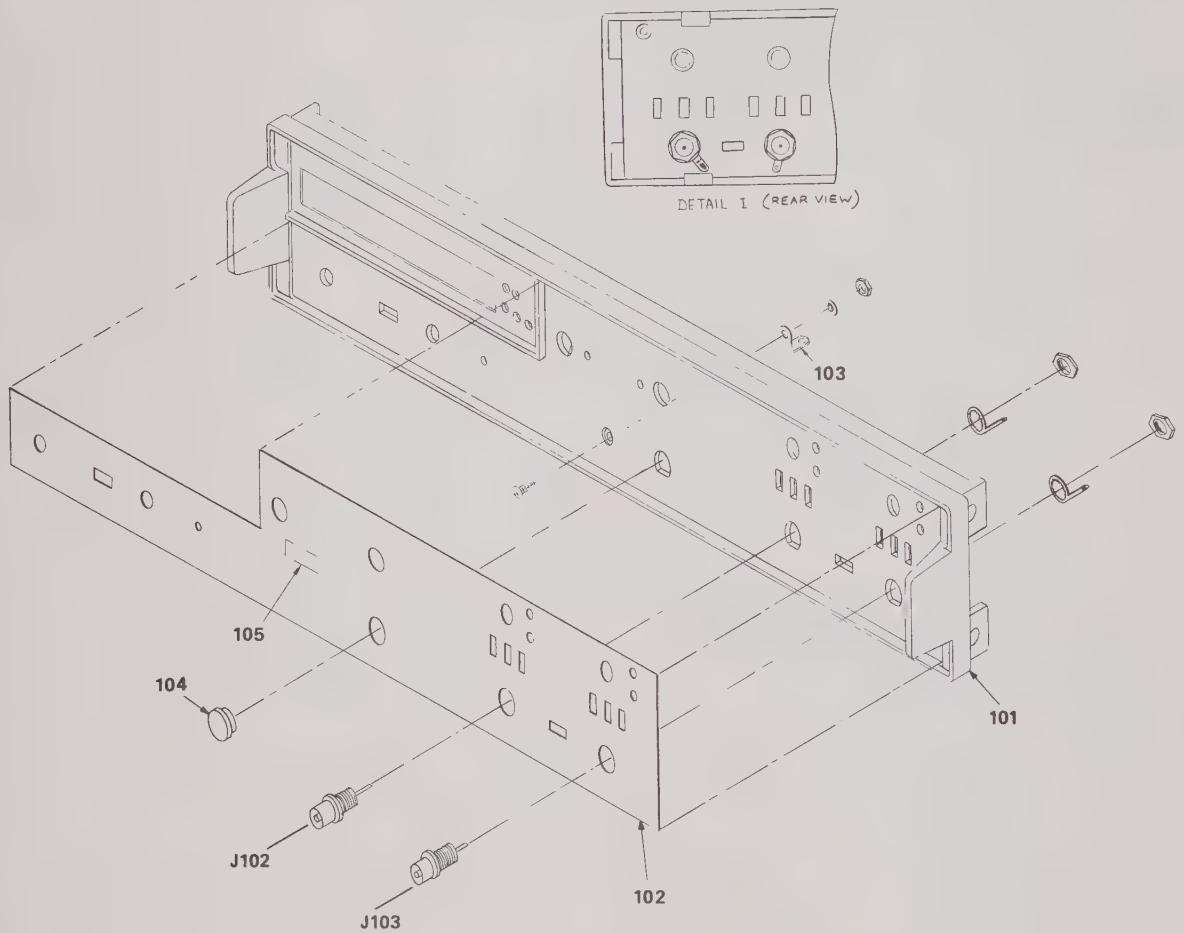
USE	
CODE	SERIAL NUMBER EFFECTIVITY

CAUTION

Indicated devices are subject to damage by static discharge.

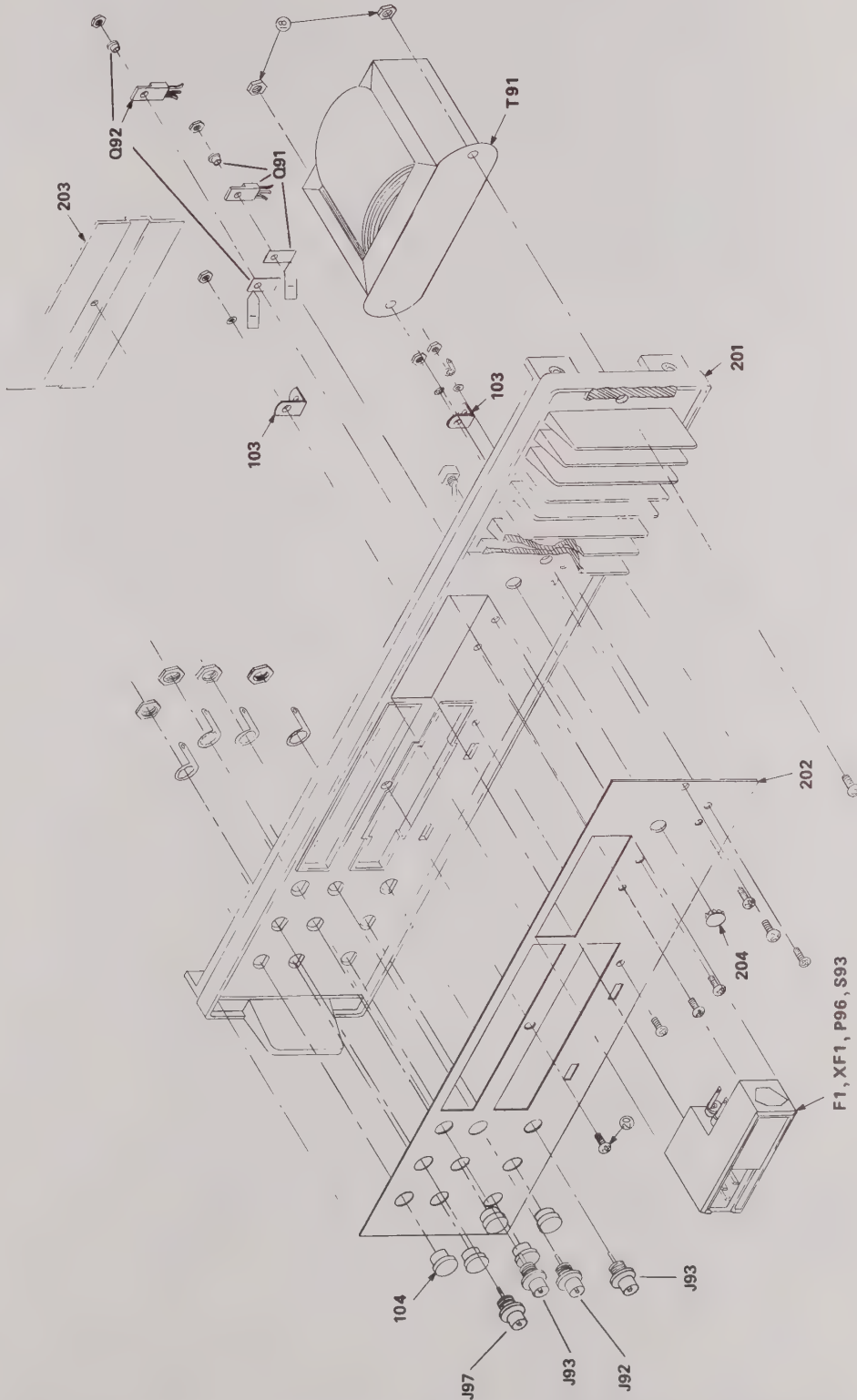
Table 5-1. Final Assembly - Model 1953A (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	FINAL ASSEMBLY (Figure 5-1 through 5-5).						
	Front Panel View (Figure 5-1)						
101	Front Panel	433516	89536	433516	1		
102	Front Panel Decal	394106	89536	394106	1		
103	Angle Bracket	401869	89536	401869	3		
104	Plug Button	398206	89536	398206	6		
105	Nameplate	393975	89536	393975	1		
J102 J103	BNC Connector	152033	13511	UG1094A/U	2		
	Rear Panel View (Figure 5-2)						
201	Rear Panel	449469	89536	449469	1		
202	Rear Panel Decal	452748	89536	452748	1		
F91	Fuse, 1 amp	369819	71400	AGC1	1		
XF91, P96, S93	Power Receptacle, fuse holder and voltage change over	446328	89536	446328	4		
J91, J92, J93, J97	BNC Connector	152033	13511	UG1094A/U	4		
Q91, Q92	Xstr, power, Si, PNP	369660	01295	T1P32	2	1	
T91	Transformer	449843	89536	449843	1		
203	Cover, basic	398024	89536	398024	1		
204	Plug, button	101766	83330	654	1		



Note: Items illustrated but not called out are common hardware.

Figure 5-1. Front Panel View

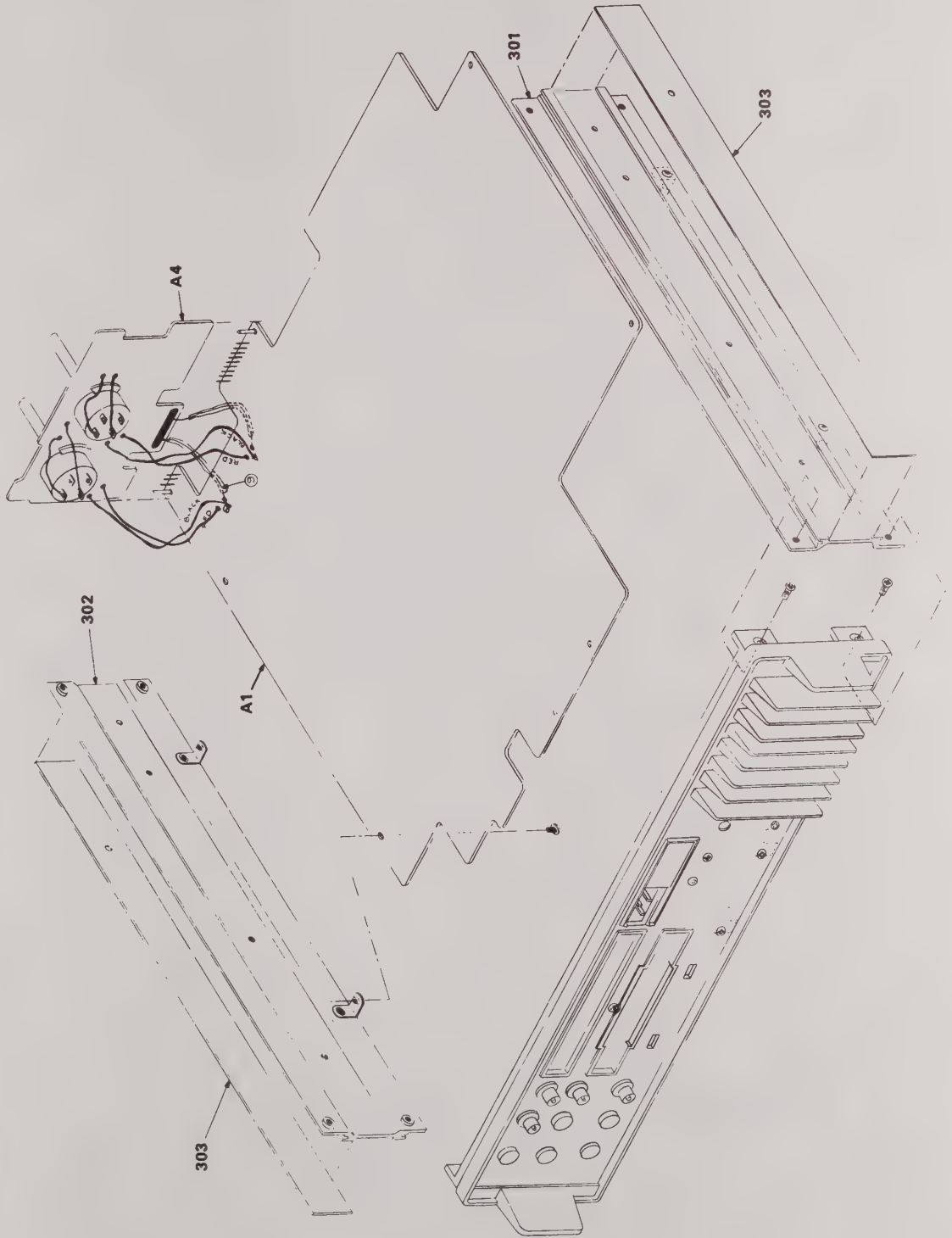


Note: Items illustrated but not called out are common hardware.

Figure 5-2. Rear Panel View

Table 5-1. Final Assembly - Model 1953A (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	Main Assembly View (Figure 5-3)						
A1	Main PCB Assembly (Table 5-2)	396200	89536	396200	1		
A4	Input PCB Assembly (Table 5-5)	396234	89536	396234	1		
301	Chassis, left side	395954	89536	395954	1		
302	Chassis, right side	395947	89536	395947	1		
303	Decal, side	401224	89536	401224	1		
	Interior View (Figure 5-4)						
A2	Display Assembly (Table 5-3)	396218	89536	396218	1		
A3	Switch Assembly (Table 5-4)	396226	89536	396119	1		
401	Know Assembly, putty grey	341388	89536	341388	2		
402	Know Assembly, pointer, putty grey	341404	89536	341404	2		
403	Know Assembly, putty grey	365015	89536	365015	1		
	Exterior View (Figure 5-5)						
501	Cover, bottom	395970	89536	395970	1		
502	Cover, top	395962	89536	395962	1		
503	Foot, Bail, Stand	292820	89536	292820	4		
504	Insert, non-skid, foot	302026	89536	302026	4		
505	Lens	395921	89536	395921	1		
506	Handle Frame	398198	89536	398198	1		
507	Grip	284836	89536	284836	2		
508	Know, female half	309054	89536	309054	2		
509	Know, male half	309047	89536	309047	2		
510	Washer, spring	228981	89536	228981	2		
511	Decal, know, spun finish	285221	89536	285221	2		
512	Line Cord (not illustrated)	343723	89536	343723	1		



Note: Items illustrated but not called out are common hardware.

Figure 5-3. Main Assembly View

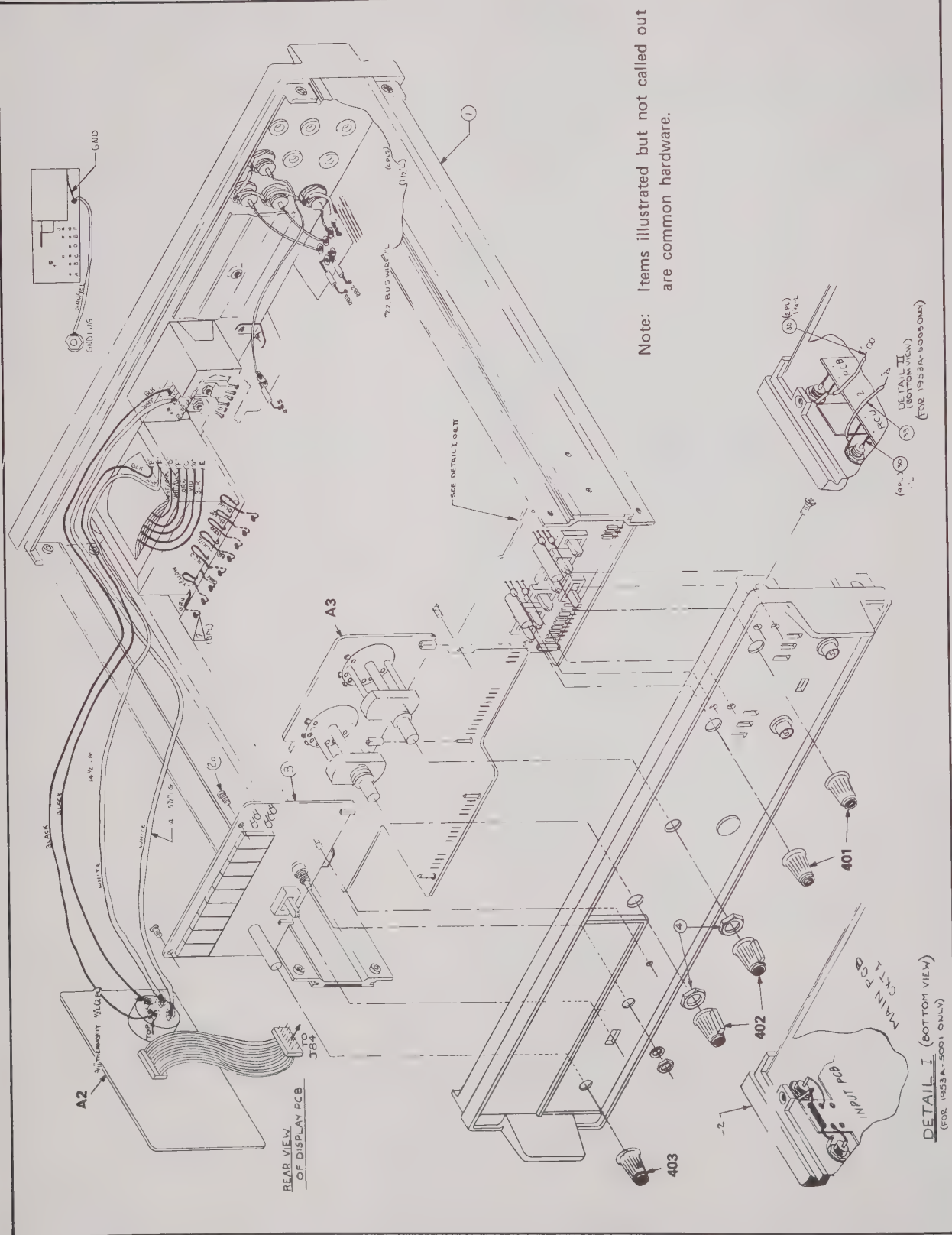


Figure 5-4. Interior View

Note: Items illustrated but not called out are common hardware.

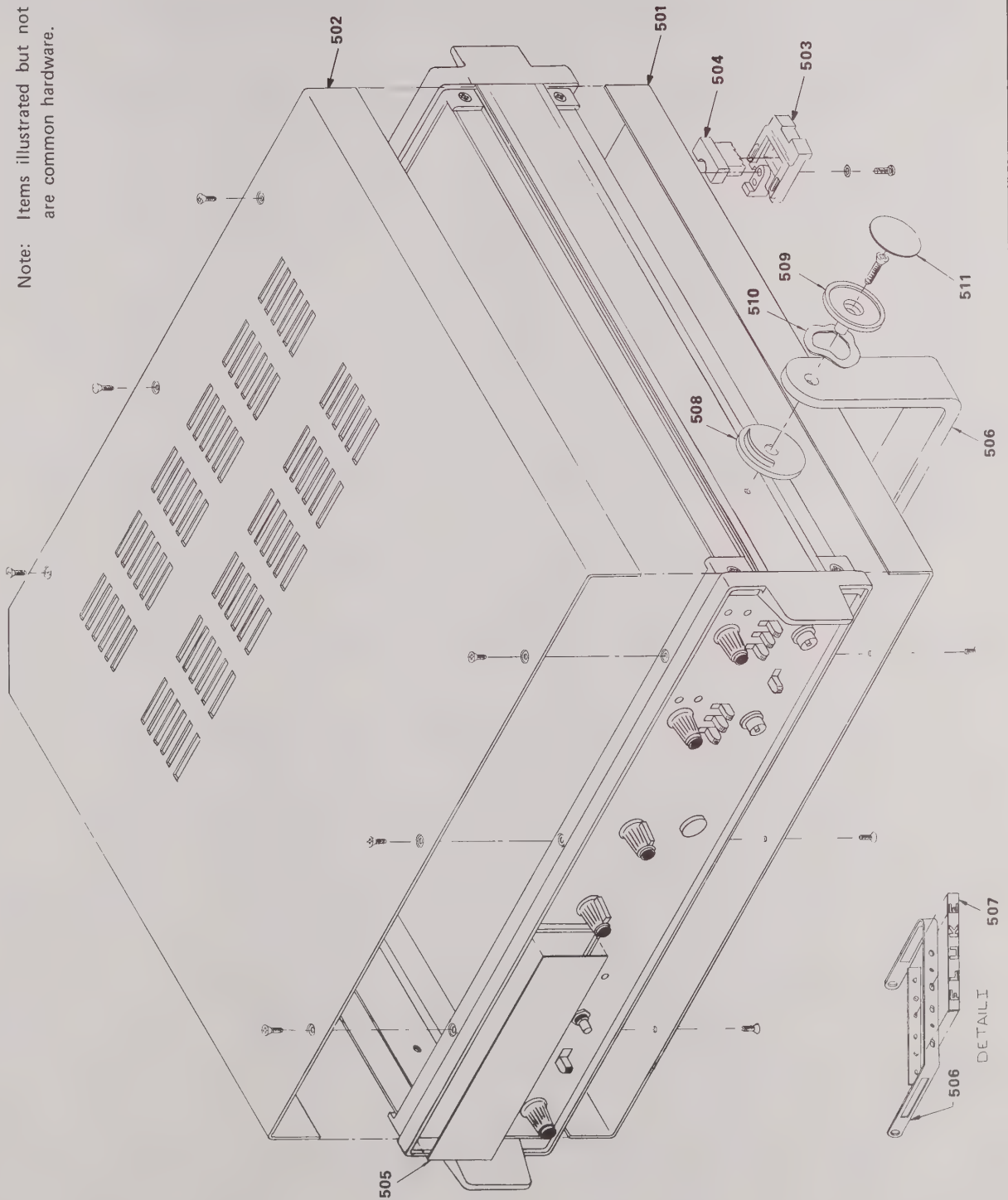


Figure 5-5. Exterior View

Table 5-2. Main PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A1	MAIN PCB ASSEMBLY Figure 5-6	396200	89536	396200	REF		
C1, C41, C56, C57	Cap, cer, disc, 47 pF $\pm 20\%$, 1000V	369132	56289	C030B102H470J	4		
C2, C4, C14, C21 C22, C24, C31, C36, C37, C38, C39, C43, C44, C54, C61, C64, C69, C76, C77	Cap, Ta 10 μ F $\pm 20\%$, 15V	193623	56289	196D106X0015 KA4	19		
C3, C42	Cap, cer 0.22 μ F, 20%, 50V	309849	71590	CW30C224K	2		
C5, C6, C32, C55, C58, C59, C60	Cap, cer, .01 μ F $\pm 20\%$, 100V	407361	72982	8121-A100-W5R- 103M	7		
C71	Cap, tant, 22 μ F, $\pm 20\%$, 25V	357780	56289	196D226X0025- PE4	1		
C73, C103, C104	Cap, cer, 1000 pF $\pm 10\%$, 500V	357806	56289	C106B102G102	3		
C75, C102	Cap, cer, disc, 10 pF, $\pm 10\%$, 3 kV	105536	56289	40C362A1	2		
C75	Cap, elect, 220 μ F, -10/+50%, 35V	369181	25403	ET221X025A00	1		
C92	Cap, elect, 470 μ F, -10/+50%, 25V	168153	73445	ET471X0025A0-1	1		
C93	Cap, elect, 1000 μ F, -10/+100%, 40V	340901	99392	39C40HH13	1		
C94, 95	Cap, elect, 4700 μ F, -10/+100% 25V	379370	99392	39CS15HLS3	1		
C96	Cap, cer, disc, 500 pF $\pm 10\%$, 500V	105692	71590	2DDH60N501K	1		
C101	Cap, cer, disc, .01 μ F, -20/+100%, 40V	369579	72982	8121-A050-651- 103Z	1		
CR1, CR4, CR41, CR44	Diode, Zener 3.3V, +5%, 28 ohms at 20mA	309799	07263	1N746A	4	1	
CR2, CR3, CR42, CR43	Diode, ultra fast lo cap, Si	381806	07263	1N3062	4	1	

Table 5-2. Main PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
CR76, CR77, CR78, CR100, CR102, CR103, CR121, CR122	Diode, Si, Hi-speed 75V, 150 mA	203323	07910	1N4448	7	2	
CR91, CR92	Diode, Si, Rectifier	187716	04713	MR1032B/1N49 99	2	1	
CR93 thru CR96	Diode, Si, 125 piv, 150mA	272252	07263	FD333	4	1	
CR101	Diode, Zener voltage reg 6.2V +5%	325811	07263	1N753A	1	1	
J81 thru J85	Socket, I.C., 16 pins	387324	91506	316G37D	5		
Q1, Q5	Xstr, dual FET N-channel, hi gfs E421	379271	17856	E421	2	1	
Q2, Q6	Xstr, sig, NPN, Si	333898	04713	MPSH10	2	1	
Q3, Q4, 4, Q7 thru Q12 Q16, Q17 Q18, Q22	Xstr, PNP, Si	369629	07263	2N5771	12	3	
Q13, Q14	Xstr, NPN, Si, lo P	369645	07263	2N4274	2	1	
Q15	Xstr, PNP, Si, lo P	369603	07263	2N4257	1	1	
Q21	Xstr, FET, N-channel	369637	01295	2N5951	1	1	
Q71, Q72, Q73, Q74 Q75, Q79, Q80 Q81, Q85, Q86 Q87, Q95	Xstr, Si, PNP	218396	04713	2N3904	12	3	

Table 5-2. Main PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
Q76, Q77, Q78, Q82, Q83, Q84, Q88, Q89, Q90, Q97	Xstr, PNP, Si	352369	12040	2N4403	10	2	
Q96	Xstr, NPN, Si	150359	07263	2N3053	1	1	
Q98	Xstr, sm sig, PNP, Si	269076	04713	2N4890	1	1	
	Heat Sink, xstr	370155	05820	204CB	1		
	Transipad	152207	07047	10123-DAP	2		
R1, R41	Res, comp, 180k $\pm 5\%$, 1/4W	193441	01121	CB1845	2		
R2, R42	Res, comp, 22 $\pm 5\%$, 1/4W	147884	01121	CB2205	2		
R3, R70, R84, R106, R121, R122	Res, comp, 1k $\pm 5\%$, 1/4W	148023	01121	CB1025	6		
R4, R44	Rex, comp, 120k $\pm 5\%$, 1/2W	108779	01121	EB1245	2		
R5, R45	Res, comp, 180 $\pm 5\%$, 1/4W	147942	01121	CB1813	2		
R6, R46, R95	Res, comp, 3.3k $\pm 5\%$, 1/4W	148056	01121	CB3325	3		
R7, R47	Res, comp, 2.7k $\pm 5\%$, 1/4W	170720	01121	CB2725	2		
R8, R9, R48, R49, R63, R75	Res, comp 470 $\pm 5\%$, 1/4W	147983	01121	CB4715	6		
R10, R50, R66	Res, comp 150 $\pm 5\%$, 1/4W	147934	01121	CB1515	3		
R11, R15, R53, R57, R68, R107	Res, comp 560 $\pm 5\%$, 1/4W	147991	01121	CB5615	6		
R12, R14, R54, R56, R64	Res, comp, 820 $\pm 5\%$, 1/4W	148015	01121	CB8215	5		

Table 5-2. Main PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R13, R21, R25, R55, R69	Res, comp, 270 $\pm 5\%$, 1/4W	160804	01121	CB2715	5		
R18, R58, R60, R65	Res, comp, 220 $\pm 5\%$, 1/4W	147959	01121	CB2215	4		
R19, R22, R24, R26, R27, R82, R83, R85	Res, comp, 100 $\pm 5\%$, 1/4W	147926	01121	CB1015	8		
R20, R51, R52, R110	Res, comp, 330 $\pm 5\%$, 1/4W	147967	01121	CB3315	4		
R23	Res, comp, 390 $\pm 5\%$, 1/4W	147975	01121	CB3915	1		
R28	Res, comp, 3.9k $\pm 5\%$, 1/4W	148064	01121	CB3925	1		
R29	Res, comp, 3.6k $\pm 5\%$, 1/4W	241620	01121	CB3625	1		
R30, R31	Res, comp, 22k $\pm 5\%$, 1/4W	148130	01121	CB2235	2		
R32, R33	Res, comp 2.2M $\pm 5\%$, 1/4W	198390	01121	CB2255	2		
R34, R35	Res, var trimpot, 10k $\pm 20\%$, 10V	369553	Piher	PF-10V-10K	2		
R36 thru R39, R94	Res, comp, 56 $\pm 5\%$, 1/4W	147900	01121	CB5605	5		
R43	Res, comp, 680 $\pm 5\%$, 1/4W	148007	01121	CB6815	1		
R59, R61	Res, comp, 240 $\pm 5\%$, 1/4W	221895	01121	CB1225	2		
R62, R71, R73, R76, R96, R98	Res, comp, 5.6k $\pm 5\%$, 1/4W	148080	01121	CB5625	6		
R67	Res, comp 1.2k $\pm 5\%$, 1/4W	190371	01121	CB1225	1		
R72	Res, comp, 47 $\pm 5\%$, 1/4W	147892	01121	CB4705	1		
R74	Res, comp, 100k $\pm 5\%$, 1/4W	148189	01121	CB1045	1		
R77	Res, comp, 2.2k $\pm 5\%$, 1/4W	148049	01121	CB2225	1		
R78, R80, R105, R123	Res, comp, 10k $\pm 5\%$, 1/4W	148106	01121	CB1035	4		
R86	Res, W.W., 0.2 ohms $\pm 5\%$, 2W	352914	75042	AS-2	1	1	
R88, R91, R92	Res, M.F. 10k $\pm 1\%$, 1/8W	168260	91637	MFF1-81002F	3		

Table 5-2. Main PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R89	Res, M.F., 14k $\pm$ 1%, 1/8W	379057	91637	MFF1-81402F	1		
R90	Res, comp, 4.7 $\pm$ 5%, 1/4W	193359	01121	CB47G5	1		
R93	Res, nkiflm, 1 ohm $\pm$ 5%, 1/4W	357665	80031	CR251-4P51E	1		
R97	Res, var trimpot, 1k $\pm$ 20%, 10V	402685	Piher	PT10V-1K	1		
R100	Res, comp, 10 $\pm$ 5%, 1/4W	147868	01121	CB1005	1		
R104	Res, comp, 1M $\pm$ 5%, 1/4W	182204	01121	CB1055	1		
R108	Res, comp, 47k $\pm$ 5%, 1/4W	148163	01121	CB4735	1		
R109	Res, comp, 1.8k $\pm$ 5%, 1/4W	175042	01121	CB1825	1		
R124 thru R127	Res, comp, 27k $\pm$ 5%, 1/4W	148148	01121	CB2735	4		
S91, S92	Switch, DPDT slide	404814	79727	G1-152-pc	2	1	
U1, U2	I.C. ECL comp, triple diff line receiver	402727	07263	F95116DC	2	1	
U3, U5	Res, network 680 $\pm$ 5%, 1/4W	402644	56289	TYPE916C	2	1	
U4	I.C. ECL triple 4-3-3 input OR gate	402735	07263	F95106DC	1	1	
U6	I.C. ECL edge triggered JK flip-flop 16 pins	402743	07263	F95029DC	1	1	
U7	Oscillator, crystal	369751	02533	X0-10000-6	1		
U11, U12, U15, U18, U19, U36, U37	I.C. TTL, MSI, dec. ctr, 14 pins	293159	01295	SN7490N	7	1	
U14, U23, U44, U45, U52, U53, U62	I.C. TTL, quad 2 input AND gate, 14 pins	292953	01295	SN7400N	7	2	
U16, U33, U58, U64	I.C. TTL, hex inv, 14 pins	292979	01295	SN7404N	4	1	
U17	I.D. TTL, decade ctr, 14 pins	293159	01295	SN7490AN	1	1	
U21	I.C. lin, differential voltage comparator	429050	12040	LM710CN	1	1	
U22	I.C. TTL, Schottky quad 2 input excl. OR gate	379297	01295	SN74S86N	1	1	
U24, U42	I.C. TTL AND-OR inverter	379289	01295	SN74S64N	2	1	
U25	I.C. TTL, dual D flip-flop	418269	01295	SN74S74N	1	1	

Table 5-2. Main PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U26, U28	I.C. TTL, quad 2 input pos OR gate	393108	01295	SN74LS32N	2	1	
U27	I.C. TTL, 8 input pos NAND, 14 pin	407338	01295	SN74S30N	1	1	
U31, U32	I.C. TTL, Schottky dual, edge triggered	363440	01295	SN74S112N	2	1	
U34, U59	I.C. TTL dual d type edge-triggered flip-flops	310227	01295	SN7474N	2	1	
U35	I.C. TTL quad 2 input pos NOR gate	403626	01295	SN74S02N	1	1	
U41, U63	I.C. TTL, triple 3 input pos NAND gate	292995	01295	SN7410N	2	1	
U43, U54, U55, U68	I.C. TTL, quad 2 input NOR gate, 14 pins	288845	01295	SN7402N	4	i	
U46	I. C. dig-TTL, quad 2 input pos OR gates Totem Pole Outputs	342709	01295	SN7432N	1	1	
U47, U56	I.C. TTL quad 2 input NAND gate with Open Coll.	292961	01295	SN7403N	2	1	
U51	I.C. TTL, 8 input pos NAND gate	293019	01295	SN7430N	2	1	
U57	I.C. TTL, decade ctr, 14 pins	320754	01295	SN74196N	1	1	
U61	I.C. TTL, hex inverter, open collector	379305	01295	SN7405N	1	1	
U65	I.C. MOS, 2.5 MHz, 7 digit decade ctr, 40 pins ⊗	380238	89536	380238	1	1	
U66	I.C. TTL dual 5 bit shift register, 16 pins	293399	01295	SN7496N	1	1	
U67	I.C. TTL dual monostable multivibrator	310235	01295	SN74123N	1	1	
U69	I.C. TTL, dual 4 input pos NAND gate	293001	01295	SN7420N	1	1	
U71, U72	I.C. TTL BCD to 7 segment decoder driver	340109	01295	SN7447N	2	1	
U73, U74	I.C. CMOS hex buffer/inverter, 16 pins ⊗	381830	95303	SD4050AE	2	1	
⊗ Indicates MOS device that may be damaged by static discharge.							

Table 5-2. Main PCB Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U81	Res, network 47 ohms $\pm 5\%$, 1/4W	402636	56289	TYPE914C	1	1	
U92	Diode Bridge 100V, 2A, full wave	296509	14936	KBF02	1	1	
U94, U95	I.C., linear, op amp A741, 8 pins	402750	07263	741TC	2	1	
U96	I.C. linear, voltage regulator, 14 pin DIP	379420	04713	MC1723C	1	1	
XU4, XU6, XU31, XU35	Socket, IC 16 pin, low profile	370312	01295	C931602	4		
XU13, XU35	Socket, I.C. 14 pin	291542	00779	582527-1	2		
XU65	Socket, I.C., 40 pin	386060	89536	386060	1		

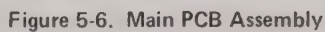


Table 5-3. Display PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A2	DISPLAY PCB ASSEMBLY Figure 5-7	396218	89536	396218	REF		
D101 thru DS108	Light Emitting Diode	385898	28480	5082-4887	8	3	
J84	Flat Cable Assembly	393520	08261	5142-006	1		
Q1	Xstr, Si, PNP	218396	04713	2N3904	1	1	
R102, S101, S131	Assy, res, var, with dpst sw, 25k	379446	89536	379446	1	1	
R103	Res, fxd, comp 10k $\pm 5\%$, 1/4W	148106	01121	CB1035	1		
R104	Res, fxd, comp, 110 $\pm 5\%$, 1/4W	193474	01121	CB1115	1		
R105	Res, fxd, comp, 3.3k $\pm 5\%$, 1/4W	148056	01121	CB3325	1		
S102	Sw Slide	380113	79727	GF-124-SPDT	1	1	
S103	SW SPST	370353	08353	8532	1	1	
U101 thru U109	Display, LED, orange	429985	28480	5082-7728	9	3	
U113	Res, network 110 $\pm 5\%$, 1/4W	386938	56289	TYPE916C	1	1	
	Receptacle	375329	00779	85863-3	12		
	Connector (Black)	149112	74970	105-0753	2		

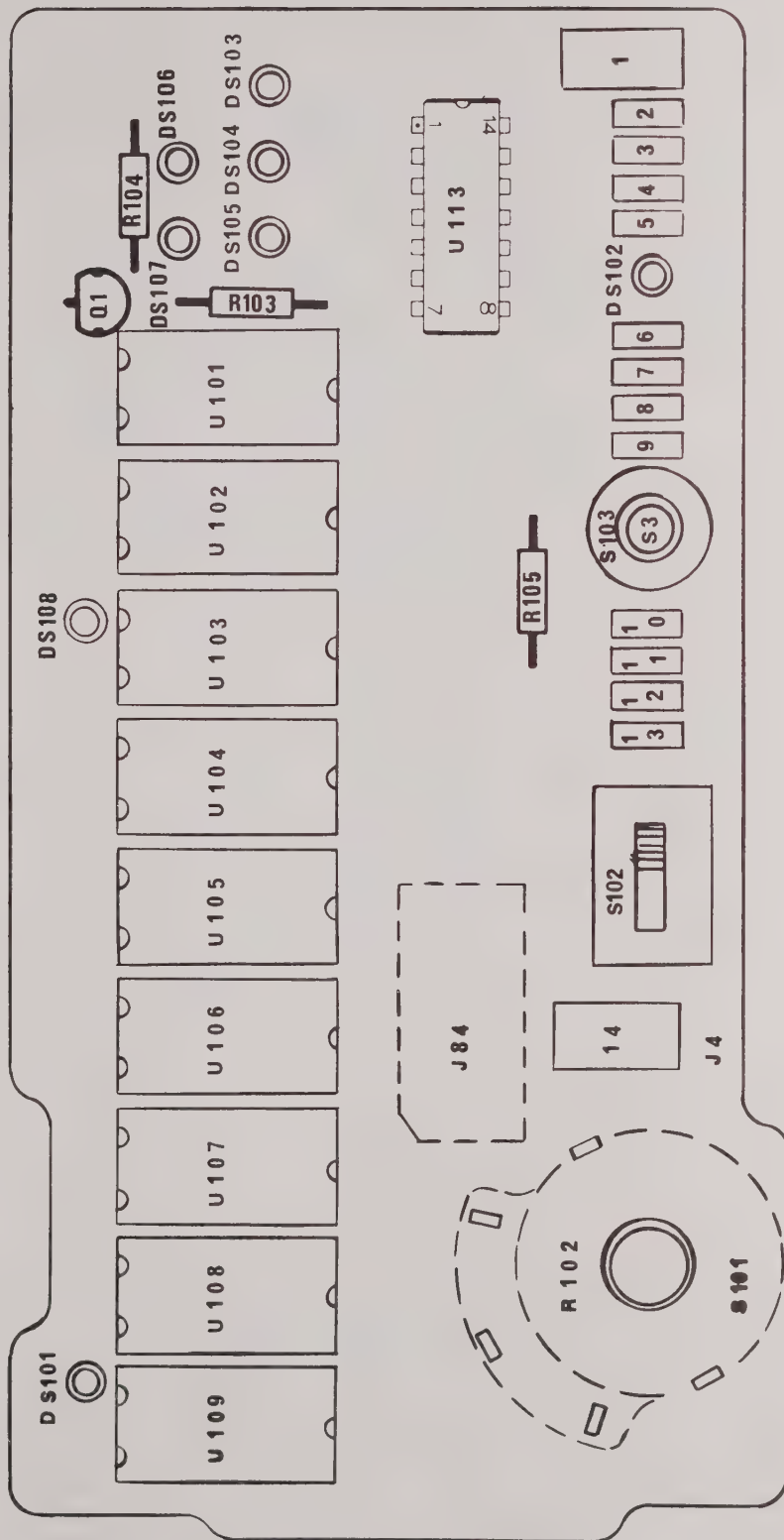


Figure 5-7. Display PCB Assembly

Table 5-4. Switch PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A3	SWITCH PCB ASSEMBLY Figure 5-8	396226	89536	396226	REF		
S104	Switch Timebase	376988	89536	376988	1		
S105	Switch Function	376970	89536	376970	1		
U301	Resistor Network 13 res, 6k $\pm 5\%$, 1/4W	355131	71450	760-1	1	1	
	Receptacle, Board mount	375329	00779	85863-3	14		
	Connector (black)	149112	74970	105-0753	2		

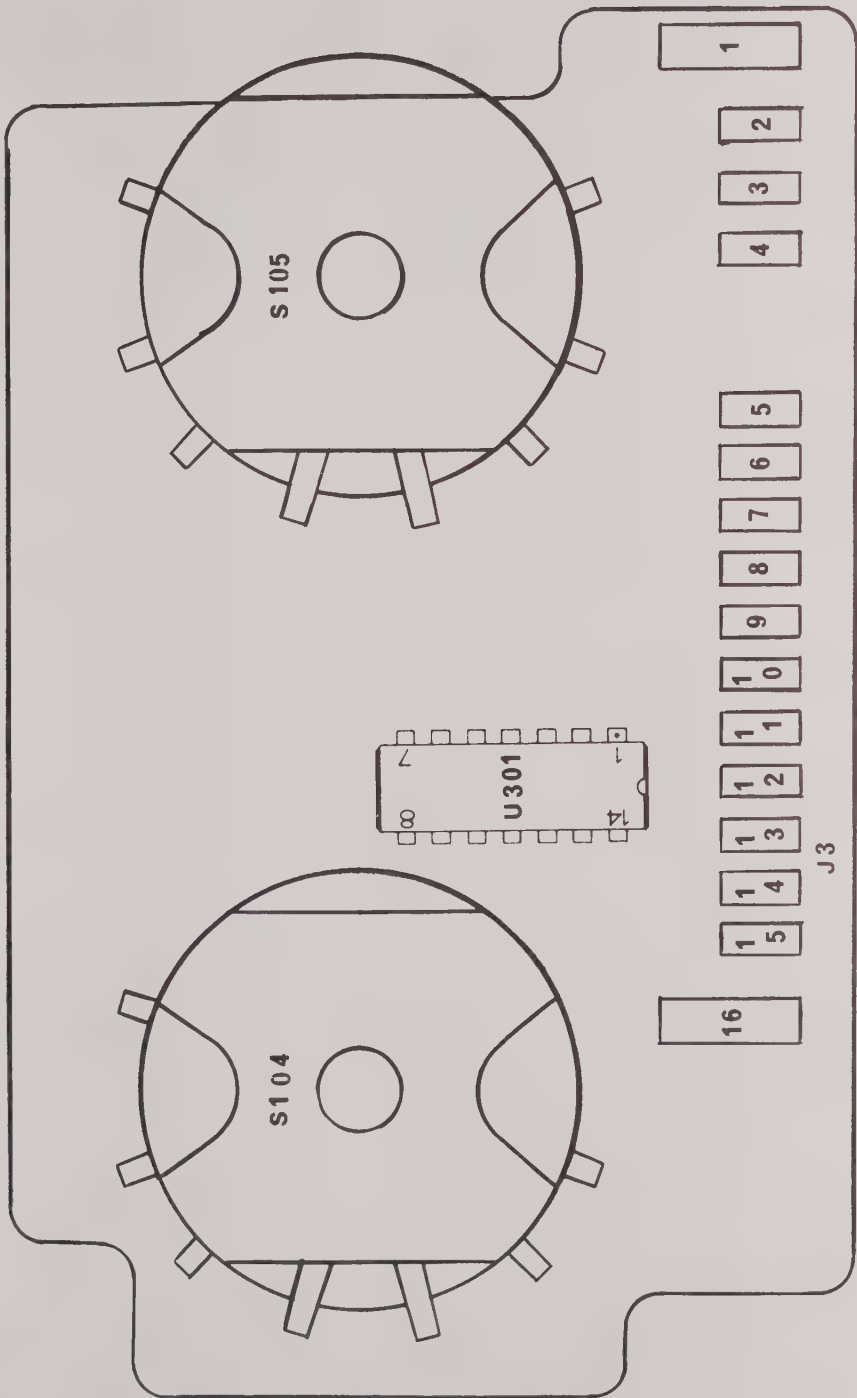


Figure 5-8. Switch PCB Assembly

Table 5-5. Input PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A4	INPUT PCB ASSEMBLY Figure 5-9	396234	89536	396234	REF		
C401, C402	Cap, mylar 0.1 ufd + 10%	161992	73445	C280AE/A100K	2		
DS401, thru DS404	Light Emitting Diode	385898	28480	5082-4887	2		
R401, R402	Res, comp, 910k $\pm 5\%$, 1/4W	285338	01121	CB9145	2		
R403, R404	Res, comp, 100k $\pm 5\%$, 1/4W	148189	01121	CB1045	2		
R405, R406	Res, var, 10k $\pm 30\%$, 1/2W switching spdt	370247	71450	FR-VF-UPE45-4	2	1	
R410, thru R413	Res, comp, 47 ohms $\pm 5\%$, 1/4W	147892	01121	CB4705	4		
R420, R421	Res, comp, 1k $\pm 5\%$, 1/4W	148023	01121	CB1025	2		
S108, thru S113	Sw Slide spdt	380113	79727	GF-124-SPDT	6	2	
S114	Sw Slide dpdt	436691	34828	GF-126	1	1	
	Receptacle	375329	00779	35863-3	12		
	Connector	149112	74970	105-0753	2		

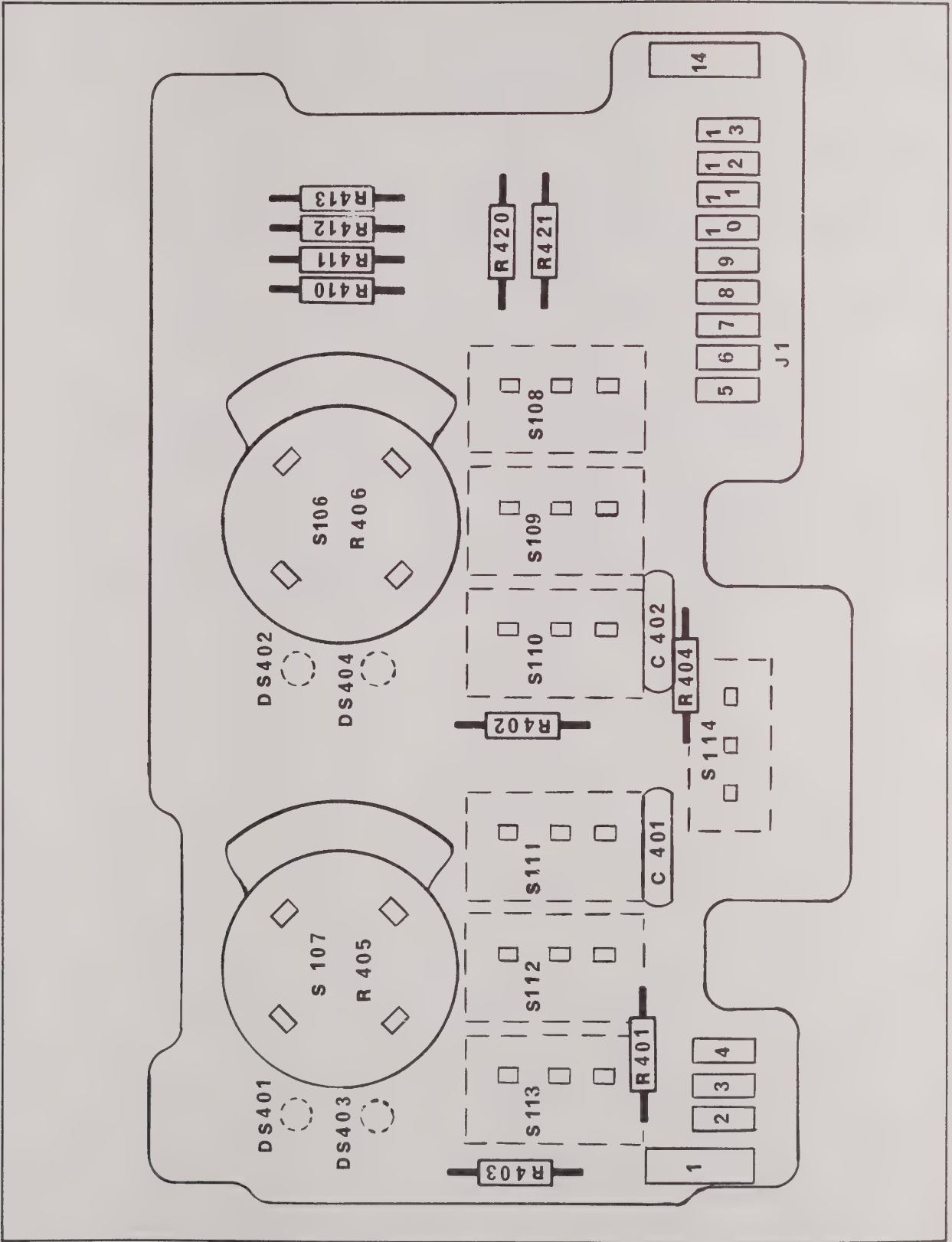


Figure 5-9. Input PCB Assembly

Section 6

Option & Accessory Information

6-1. INTRODUCTION

6-2. This section of the manual contains information pertaining to the accessories and options available for your instrument.

6-3. ACCESSORY INFORMATION

6-4. The accessory information, if applicable, will contain details concerning accessories that may be used with this particular instrument.

6-5. OPTION INFORMATION

6-6. Each of the options available for this instrument if any, are described separately under headings containing the option number. The option descriptions contain applicable operating and maintenance instructions and field installation procedures. A complete list of replaceable parts for each option is contained at the end of that option description.

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ACCESSORIES

600-1. Accessories available for the Model 1953A are two separate rack mounting kits for mounting the instrument in a standard 19-inch equipment rack and an extender cable kit for the IEEE Interface, Option -15.

600-2. One kit contains chassis slides and has the kit number M00-200-626. The other kit is for mounting without

slides and can be ordered with kit number M00-200-622.

600-3. The IEEE Interface Option consists of two pcb boards stacked and installed parallel to the main pcb. To increase the limited access to the center board and main pcb an extender cable kit is available which allows operation with the interface placed outside the instrument. The kit is available by ordering kit number 1953A-7020K.

Option —02 Data Output Unit

602-1. Introduction

602-2. The data output unit (DOU) permits the Model 1953A to operate in a systems environment where electrical acquisition of the measurement data is necessary. The option comprises a single pcb assembly which mounts within the 1953A case and provides all nine digits of measurement data (in BCD format), units indication, decimal point, positioning and control signals to the external system by a pcb connector accessible through the rear panel. The DOU option may be ordered at the time of purchase or may be purchased at a later date and field-installed as described in paragraph 602-3. The model number of the DOU when ordered as a field-installable kit is 1953A-02K.

602-3. Installation

602-4. The 1953A-02K DOU kit comprises the following items:

- a. DOU pcb assembly, part no. 296283.
- b. Set of four stand-offs.
- c. Mounting hardware.

602-5. Install the DOU as follows:

- a. Remove the top and bottom dust covers. Remove the upper cover plate from the rear panel.
- b. Attach the four stand-offs to the under side (non-component side) of the DOU pcb.
- c. Position the DOU down on the main pcb in the position shown in Figure 602-1 so that the stand-offs align with the matching holes in the main pcb.
- d. Secure the DOU stand-offs to the main pcb from the underside.
- e. Connect the DOU cable assemblies to the main pcb so that J83 connects to J83 and J85 connects to J85 as shown in Figure 602-1.

602-6. Data Output Format.

602-7. The DOU output is available via the upper rear panel connector, labeled BCD OUTPUT. The output data is in positive-true BCD format, TTL compatible and is transferred to the external device by means of an interconnecting cable used with the Fluke Model 2010A Digital Printer is called the 2010A-7000 and is available from the factory.

602-8. To fabricate a cable assembly for any other application, use a 50-pin connector made up of the following items:

- a. Connector body, AMP part no. 1-583717-1.
- b. Connector pins (50), AMP part no. 583616-5.
- c. Connector backshell, Fluke part no. 398005.
- d. 50-conductor cable.

602-9. The type and length of cable used is not critical since the measurement data is static. However, loading of the signals at the recording device must be TTL compatible, with fan-in less than 2. Refer to Table 602-1 for the particular pin assignments at the DOU output. The DOU output connector is numbered/lettered from A to C from left to right (as viewed from the rear) on the top side of the pcb, and from 1 to 25 from left to right on the underside of the pcb. All data is positive-true TTL compatible. The decimal point information is binary-coded to permit the six different decimal point positions to be indicated on the three available output lines (i.e. pins 1, 2 and A). Refer to Table 602-2 for the decimal point decoding.

602-10. The DOU connector also provides for an external reset input at pin 24. A logic low (ground) signal on this line resets all counter functions except the DOU itself. The DOU ready command is a low true pulse having a duration of 1.5 milliseconds, and signifies that the measurement data is stored in the DOU and ready for transfer. (When connected back to the external reset input, the DOU ready command causes the 1953A to operate in a continuous

mode, and at optimum speed, to drive a printing device.) The print command is a positive (or high) true signal of one millisecond duration to activate the printing or data logging device.

602-11. List of Replaceable Parts.

602-12. Table 602-3 is a list of replaceable parts for Data Output Unit. Refer to Figure 602-2 for component locations. Refer to Section 5 for an explanation of the columnar entries.

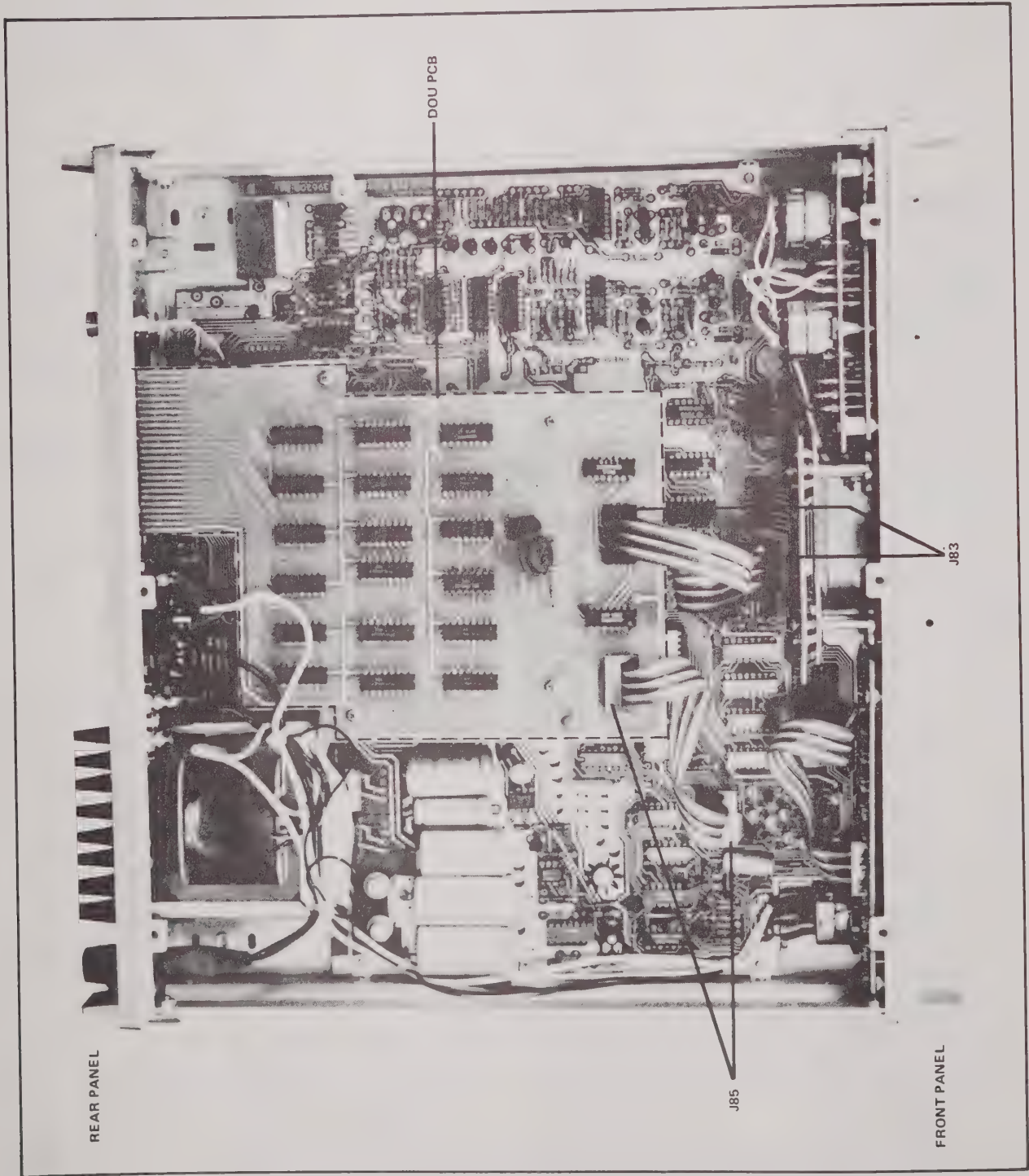


Figure 602-1. DOU Option Installed Position

Table 602-1. DOU Output Data Format

PIN NO.	FUNCTION	PIN NO.	FUNCTION
A	Decimal point 3	1	Dimension less*
B	Decimal point 1	2	Decimal Point 2
C	MHz units	3	Print
D	Milliseconds	4	kHz units
E	Seconds	5	Microseconds
F	MSD – BCD 1	6	MSD – BCD 2
H	MSD – BCD 4	7	MSD – BCD 8
J	2SD – BCD 1	8	2SD – BCD 2
K	2SD – BCD 4	9	2SD – BCD 8
L	3SD – BCD 1	10	3SD – BCD 8
M	3SD – BCD 4	11	3SD – BCD 8
N	4SD – BCD 1	12	4SD – BCD 2
P	4SD – BCD 4	13	4SD – BCD 8
R	5SD – BCD 1	14	5SD – BCD 2
S	5SD – BCD 4	15	5SD – BCD 8
T	6SD – BCD 1	16	6SD – BCD 2
U	6SD – BCD 4	17	6SD – BCD 8
V	7SD – BCD 1	18	7SD – BCD 2
W	7SD – BCD 4	19	7SD – BCD 8
X	8SD – BCD 1	20	8SD – BCD 2
Y	8SD – BCD 4	21	8SD – BCD 8
Z	LSD – BCD 1	22	LSD – BCD 2
a	LSD – BCD 4	23	LSD – BCD 8
b	Overflow	24	External Reset
c	Ground	25	DOU Ready

Table 602-2. Decimal Point Position Coding

DECIMAL POINT POSITION ON DISPLAY	DECIMAL POINT OUTPUT LINES		
	(PIN A)	(PIN 2)	(PIN B)
XXXXXXXXXX	1	1	1
XXXXXXXXXX.X	1	1	0
XXXXXXXXXX.XX	1	0	1
XXXXXXXXXX.XXX	1	0	0
XXXXXX.XXXX	0	1	1
XXXXX.XXXXX	0	1	0
XXX.XXXXXX	0	0	1
Goes high in FREQ (A/B), A GTD By B, and SELF CHECK functions			

Table 602-3. Digital Output Unit

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	DIGITAL OUTPUT UNIT Option 02						
	DOU PCB Assy (Table 602-4)	396283	89536	396283			
	Option Rear Cover	398016	89536	398016			
	Connector Kit	410241	89536	410241			

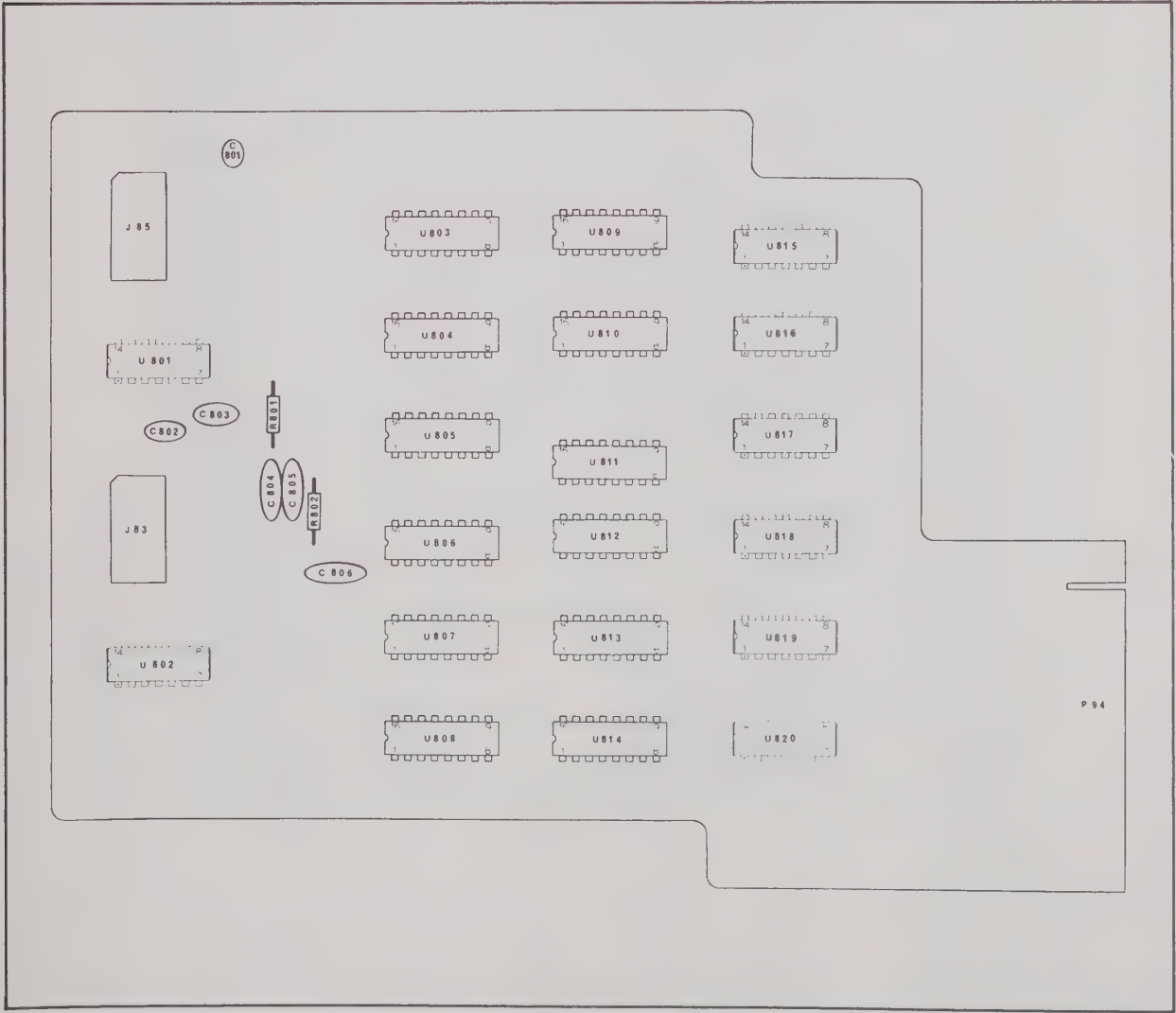


Figure 602-2. DOU PCB Assembly

Table 602-4. DOU PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	DOU PCB ASSEMBLY Figure 602-2	396283	89536	396283	REF		
C801	Cap, ta, 10 μ f $\pm$ 20%	193623	56289	196D106X0015- JA1	1		
C802	Cap, cer disc, 100 pf $\pm$ 10%, 1 kV	105593	71590	DD-101	1		
C803	Cap, cer disc, 0.01 μ f +80/-20, 16V	368639	71590	UK-16-103	1		
C804, C805, C806	Cap, cer disc, 0.1 μ f $\pm$ GHV, 25V	369199	71590	UK-25-104	3		
J83, J85	Flat Cable Assembly	393520	08261	5142-006	2		
R801	Res, comp 47k $\pm$ 5%, 1/4W	148163	01121	CB4735	1		
R802	Res, comp, 33k $\pm$ 5%, 1/4W	148155	01121	CB3335	1		
U801	IC, CMOS, triple 3 input NAND gate  14 pin	375147	95303	CD4023AE	1		
U802	IC, TTL, triple 3 input pos NOR	392951	01295	SN7427	1		
U803, U804, U805, U809 thru U814	I.C., CMOS, quad clocked d-latch  type 4042	355149	95303	CD4042AE	9		
U806	I.C. TTL, dual monostable multibibrator	310235	01295	SN74123N	1		
U807, U808	I.C., CMOS, hex buff/inv 16 pin 	381848	95303	CD4049AE	2		
U815 thru U820	I.C. TTL hex inv 14 pin	352039	01295	SN74L04	6		
 Indicates MOS device which may be damaged by static discharge.							

Option —04 TCXO

604-1. Introduction

604-2. Option -04 is a Temperature Compensated Crystal Oscillator which exhibits stability and temperature dependent characteristics which are superior to the oscillator normally installed in the standard unit. The specifications for the -04 Option are included in Section 1 of this manual.

604-3. List of Replaceable Parts

604-4. Parts for Option -04 consist only of the TCXO which replaces the standard oscillator U7. Replacements can be ordered using the Fluke Part No. 369769. The manufacturing Federal Supply Code is 89536 and the manufacturers part no. also 369769.

Option —05 External Timebase Multiplier

605-1. INTRODUCTION

605-2. The External Timebase Multiplier Option adds two operating features to the 1953A Counter-Timer. External reference inputs of 1, 5, or 10 MHz, having a minimum amplitude of 250 mVrms, may be substituted for the internal timebase reference of the instrument. Burst (pulsed oscillator) measurements may be made using control circuitry on the —05 Option.

605-3. The original External Timebase Multiplier Option has been superseded by an updated design, both of which will be covered in this section of the manual. The original version is contained on a single pcb. The later design consists of two pcbs, one mounted on the other, and is installed in instruments with serial numbers 615000 or greater (main pcb revision letter R-1 and on). The later design (two pcb version) is covered first. This information is applicable to the original version (single pcb) with the exceptions of the Timebase Multiplier theory of operation, parts list, and component location drawing, which will be covered second. Schematic diagrams for both versions are contained in Section 8.

605-4. OPERATING NOTES

605-5. External Timebase

605-6. To substitute an external reference frequency for the internal timebase, the desired input frequency (1, 5, or 10 MHz) must be selected with a three-position slide switch located on the External Multiplier pcb. Refer to Section 4 for internal access information. Apply the reference signal to the CLOCK IN connector. The EXT/INT switch controls which timebase is used in the instrument: EXT for external, INT for internal.

605-7. Burst Measurement

605-8. The burst measurement feature allows measurement of the frequency of pulsed oscillator signals within the frequency measurement capability of the instrument. Burst frequency measurements are made by selecting a

gate time for the counter of shorter duration than the pulse width of the signal to be measured. The gate time is initiated or triggered by a transition on channel B. If this transition is due to the start of the burst, and the gate time is shorter than the burst pulse width, the frequency developed during the burst is measured or counted. Burst frequency measurements made in this manner are accurate only if the pulsed oscillator being measured is not “pulled” in frequency by the start of the pulse.

605-9. There are three procedures for using the 1953A with the —05 Option to measure burst frequencies. Select one of the following procedures according to the frequency range of the unknown burst frequency.

605-10. Unknown burst frequency less than 25 MHz

- a. Select the FREQ A function and apply the unknown burst frequency to channel A.
- b. Select BURST on the rear panel switch.
- c. Select a gate time less than the width of the burst.
- d. Select COM on the SEP/COM front panel switch.
- e. Adjust channel A and channel B trigger levels for satisfactory triggering, i.e., a stable display.
- f. The counter displays the burst frequency.

605-11. Unknown burst frequency between 25 MHz and 125 MHz.

- a. Select the FREQ A function and apply the unknown burst frequency to channel A.
- b. Select BURST on the rear panel switch.
- c. Select a gate time less than the width of the burst.
- d. Apply a trigger signal at the burst repetition rate to channel B. The trigger should coincide with the start of the burst but must not start before the burst. The pulse width of the trigger does not

need to be as wide as the burst, only wide enough to trigger channel B.

- e. Adjust channel A and channel B trigger levels for satisfactory triggering, i.e. a stable display. The slope adjustment on channel B must be set at the polarity of the trigger, e.g. + slope for a positive trigger.
- f. The counter displays the burst frequency.

605-12. Unknown burst frequency greater than 125 MHz

- a. Select the **FREQ C** function and apply the unknown burst frequency to channel C.
- b. Perform steps b. through f. in paragraph 605-11 above.

605-13. THEORY OF OPERATION

605-14. External Timebase Multiplier

605-15. This description of the theory of operation for the External Timebase Multiplier portion of the —05 Option pertains only to the updated version (2 pcbs). Refer to Figure 605-1. Timebase frequency inputs to the multiplier pcb are switch selectable between internal (10 MHz) or external (1, 5, or 10 MHz). The timebase frequency is applied through U3 to a decade counter, U2 (board 1), wired for $\div 5$ and $\div 10$. The undivided input and the $\div 5$ and $\div 10$ outputs from U2 are applied to a data selector/multiplexer, U1 (board 1), which is programmed by three sections of U3 (board 1) for a 1 MHz output. The three NOR gates of U3 (board 1) used to program U1 are controlled by S1 (board 1) and SW + 12 (J6 pin 8). SW + 12 is grounded for EXT (rear panel EXT/INT switch) and is at +12V for INT. When INT is selected, the three outputs from U3 go low programming U1 for the D0 input which is the $\div 10$ output of U2. When EXT is selected, S1 controls which of the three outputs will be high to program U1 for either the D1 input ($\div 1$), the D2 input ($\div 5$), or the D4 input ($\div 10$) so there will always be a 1 MHz output from U1 (Board 1).

605-16. On board 2, the 1 MHz output from U1 (board 1) is multiplied to 10 MHz using a phase-locked oscillator. U3 is a phase comparator with the 1 MHz from board 1 applied to the reference input. The output of U3 controls the frequency of oscillation of U1. U1 oscillates at 10 MHz which is divided by a decade divider, U2, for application to the variable input of U3. The output of U1 (board 2) is used as the reference timebase for the counter. Inside U3 are three operational blocks: a digital phase detector, a charge pump, and an amplifier. Pins 2 and 11 connect the output of the phase detector, D1 (1 MHz pulses), to the input of the charge pump, PD. The

output of the charge pump, DF, is a pulse train whose average value increases or decreases to increase or decrease the frequency of the oscillator, U1. DF is connected to the input of the amplifier, A, through R4. The output of the amplifier is applied to the VTUNE input of U1. R4, R2, C4 and R5 make the amplifier an active integrator to average the output of the charge pump. R1 and C3 provide additional filtering. R3 sets the phase detector pulse width to a finite value to maintain loop gain.

605-17. BURST MEASUREMENT CONTROL

605-18. This portion of the Theory of Operation applies to both versions of the External Timebase Multiplier. Burst measurement operations are controlled by a D flipflop, U4, and four NAND gates, U5, located on board 1. When normal operation is selected with the BURST/NORMAL rear panel switch, a low is applied to one input of U5-11 through J6 pin 9. U5-11 goes high and U5-8 goes low putting U4 in the preset condition (U4-5 high) enabling U5-3 to pass the 10 MHz reference frequency. When BURST is selected, J6 pin 9 is high and either Channel A or C must be selected producing a high at J6 pin 5 (A + C). U5-11 goes low and U5-8 goes high removing the preset condition from U4. At the end of a measurement, READY (J6 pin 2) goes low, clearing U4. U4-5 goes low inhibiting the reference frequency by placing a low on one input of U5-3. When the 1953A is ready for another measurement, READY goes high. The first negative transition on XB (derived from the Channel B input) clocks U4-5 high enabling U5-3 to pass the reference frequency. When the measurement is complete, READY goes low, inhibiting the reference frequency.

605-19. PARTS LIST

605-20. Table 605-1. gives a parts breakdown for the updated version (2 pcbs) of the External Timebase Multiplier.

605-21. THEORY OF OPERATION

605-22. This portion of the Theory of Operation pertains to the early version (single pcb) of the External Timebase Multiplier. Burst Measurement theory is the same. Refer to Figure 605-2.

605-23. The timebase multiplier is a phase-locked loop oscillator that phase locks a 1 MHz, 5 MHz or 10 MHz external reference signal to the 10 MHz signal required for timing applications within the counter. As selected by the INT/EXT switch either the internal 10 MHz or an external timebase (1 MHz, 5 MHz or 10 MHz) is applied to one input of the digital comparator (U606) and to one input of U603A (see figure 605-1). With INT and NORMAL selected to enable U603A and U605D respectively, the 10 MHz internal signal is passed directly to the counter circuits. With EXT selected the

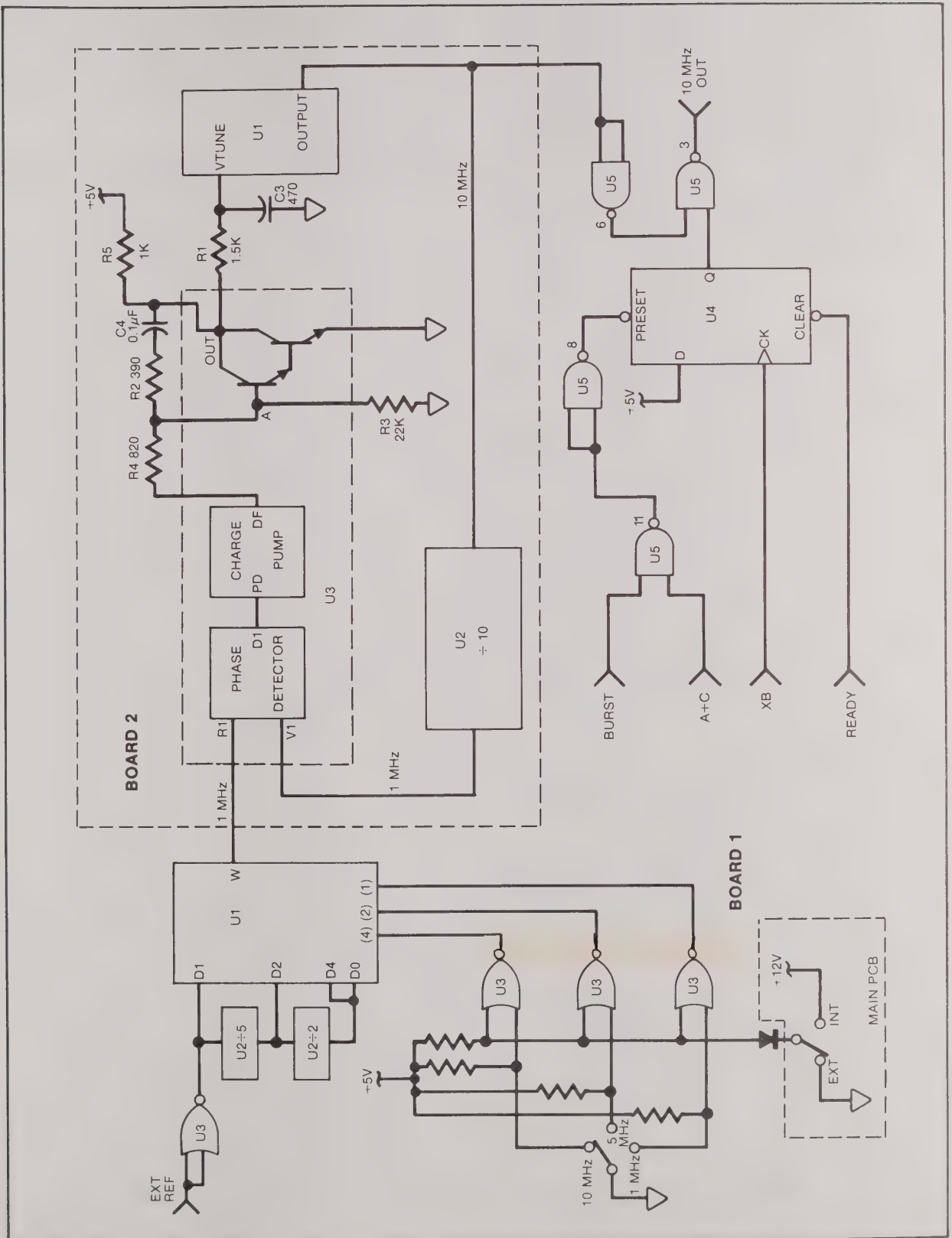


Figure 605-1. External Timebase Multiplier

external timebase reference is input to the comparator (U606) where it is phase compared against a feedback signal output from the VCD (U601). The feedback signal, depending on the position of the pcb mounted switch, is either fed directly to the comparator, or through the divider (U602) to match it to the input reference. Any difference in frequency between the external reference and the feedback signal results in an output from the comparator. This output is filtered and the correction applied to the VCO to bring the system back into phase

locked condition. The result is a 10 MHz reference applied to one input of U603C. The other input was previously enabled by the EXT switch so the reference frequency is applied to the counter circuits through U603B and U605D.

605-24. PARTS LIST

605-25. Table 605-2. gives a parts breakdown for the early version (single pcb) of the External Timebase Multiplier.

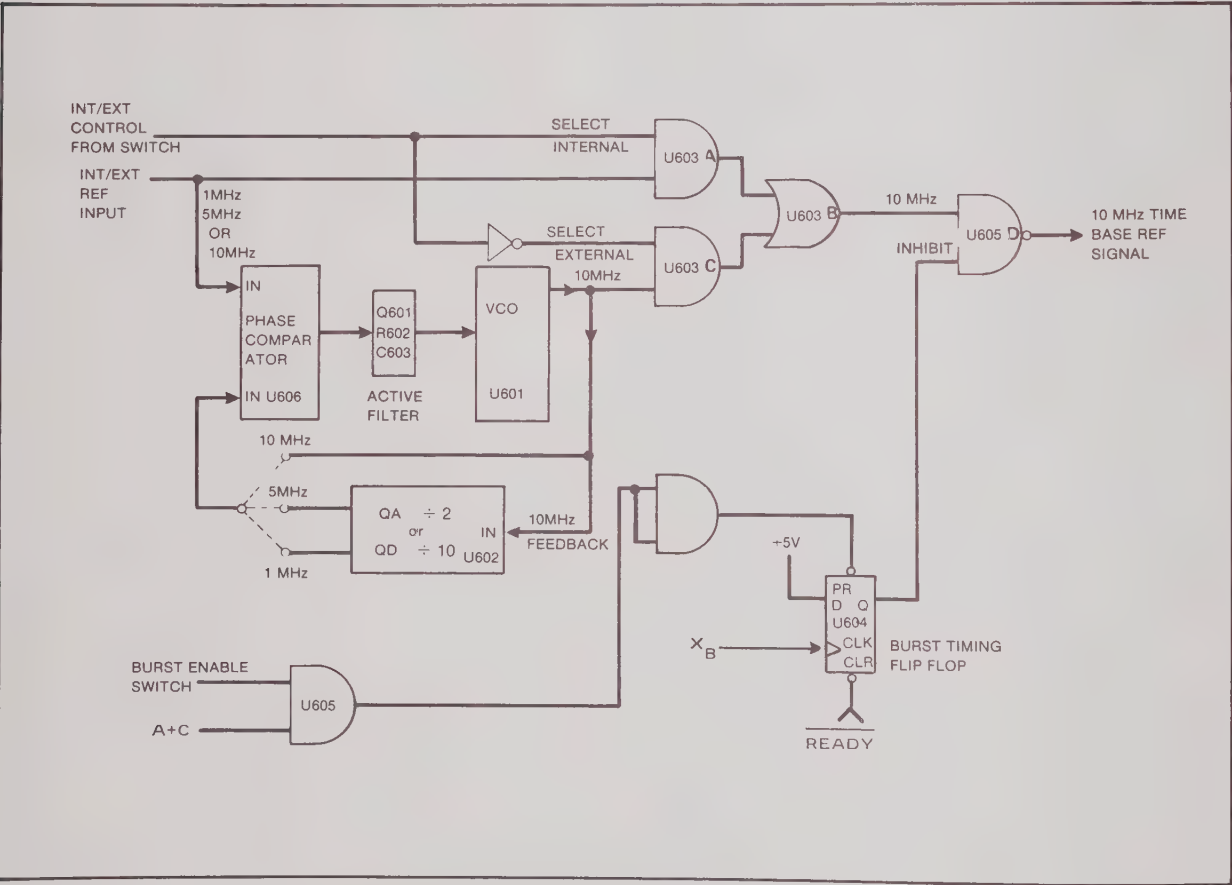
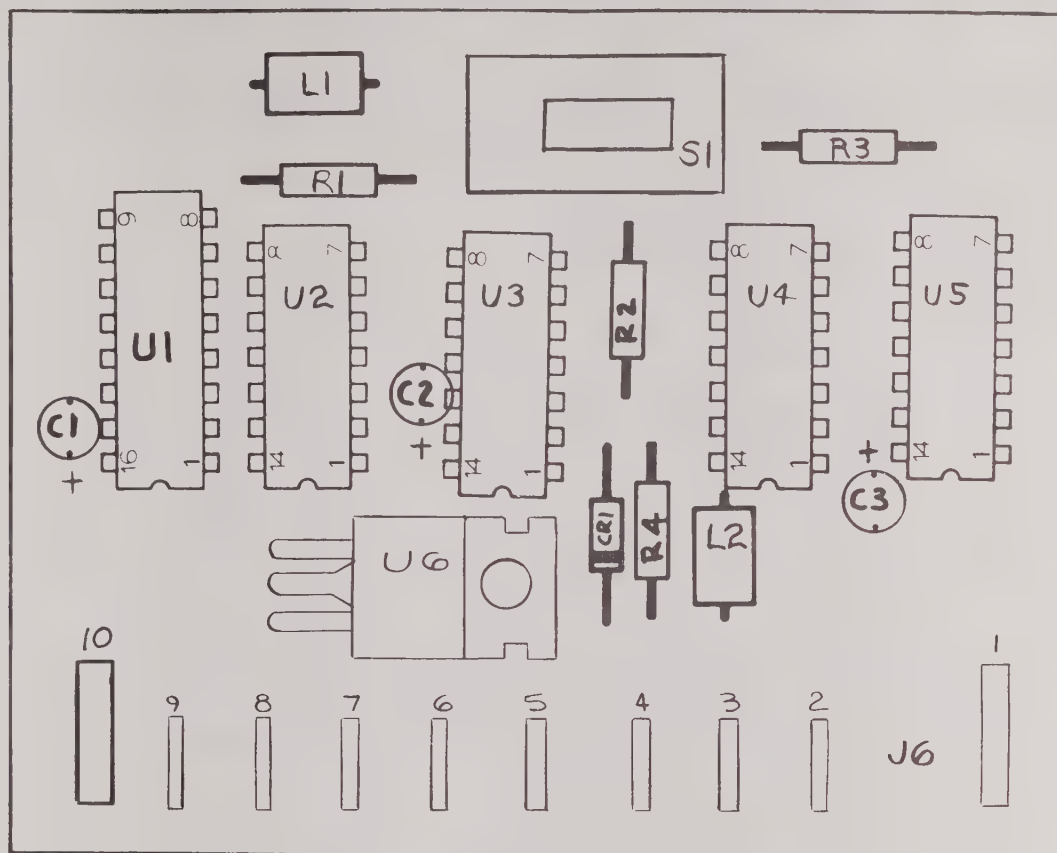
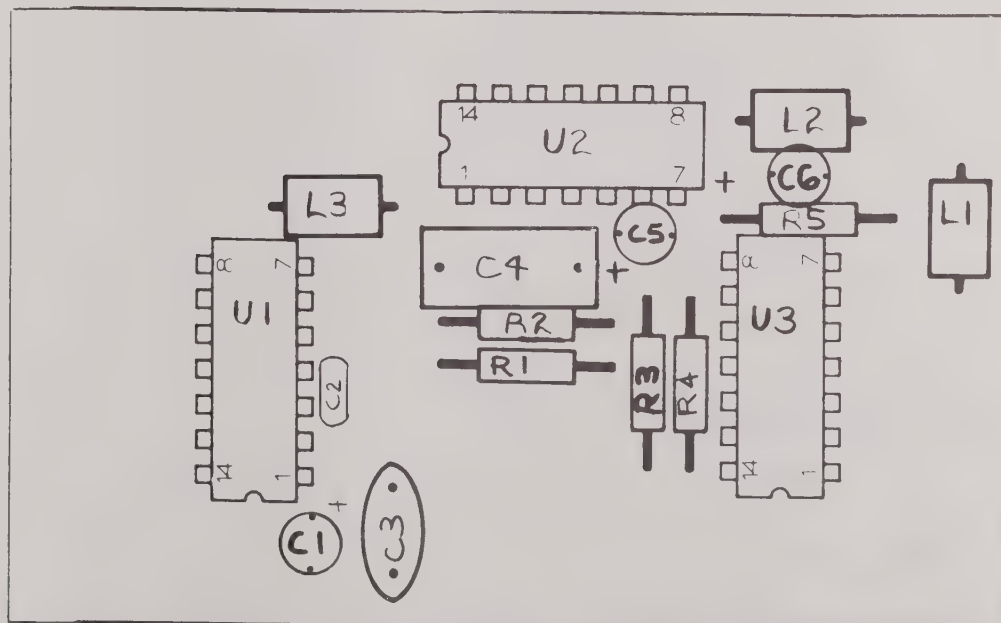


Figure 605-2. External Timebase Multiplier (Early)



External Timebase Multiplier 1



External Timebase Multiplier 2

Figure 605-3. External Timebase Multiplier (Updated)

Table 605-1 External Timebase Multiplier PCB Assembly —05 Option

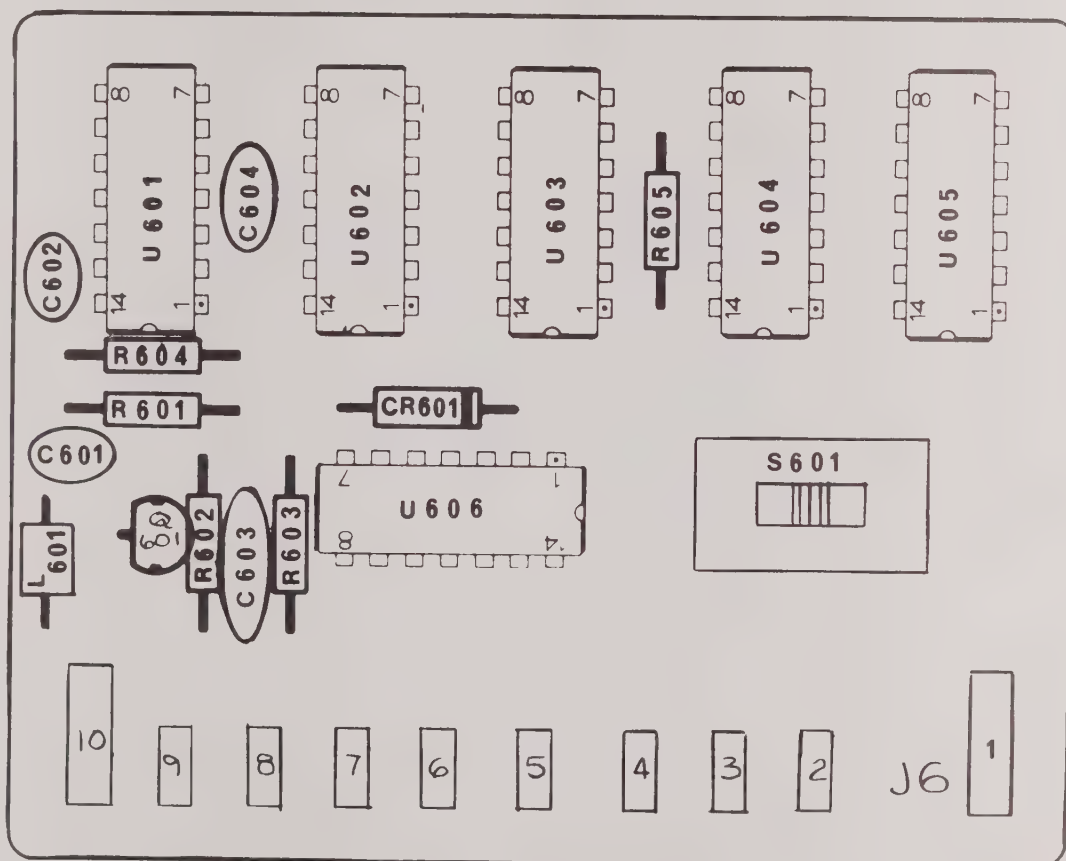
REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	EXTERNAL TIMEBASE MULTIPLIER ASSEMBLY —05 OPTION (UPDATED)						
	External Timebase Multiplier 1, PCB Assembly	467639	89536	467639	1		
	External Timebase Multiplier 2, PCB Assembly	467803	89536	467803	1		
	EXTERNAL TIMEBASE MULTIPLIER 1, PCB ASSEMBLY Figure 605-3	467639	89536	467639	REF		
C1, C2, C3	Cap, Ta, 10 μ F $\pm$ 20%, 15V	193623	56289	196D106X0015KA1	3		
CR1	Diode, Si Hi-switch	203323	07910	1N4448	1	1	
J6	Conn, jack	149112	74970	105-0753	2		
J6	Conn, receptacle	375329	00779	85863-3	8		
L1, L2	Inductor, bead, 6 turn	320911	89536	320911	2		
R1 thru R4	Res, comp, 4.7k $\pm$ 5%, 1/4W	148072	01121	CB4725	4		
S1	Switch, slide dp3t	453183	34828	G-128-L	1		
U1	IC, Dgtl, TTL, low-pwr, data selector/multiplexer	393173	01295	SN74LS151	1	1	
U2	IC, Dgtl, TTL, msi decade counters	402545	01295	SN74LS90N	1	1	
U3	IC, Dgtl, pos, NOR gates w/totem pole outputs	393041	01295	SN74LS02N	1	1	
U4	IC, Dgtl, TTL, dual D-type edge/triggered Flip-flops	310227	01295	SN7474N	1	1	
U5	IC, Dgtl, TTL, POS NAND gates	393033	01295	SN74LS00N	1	1	
U6	IC, Lin, V-regulator	355107	04713	MC7805PC	1	1	
	EXTERNAL TIMEBASE MULTIPLIER 2, PCB ASSY Figure 605-3	467803	89536	467803	REF		
C1	Cap, ta, 10 μ F $\pm$ 10%, 15V	193623	56289	196D106X-0015KA1	3	1	
C2	Cap, cer, 27 pF $\pm$ 2%, 100V	362749	72982	8121-A100-C0G-270G	1		
C3	Cap, cer, 470 pF $\pm$ 10%, 1000V	368613	71590	DD471	1		
C4	Cap, polyester film, 0.1 μ F $\pm$ 10%, 100V	393439	73445	C280MAH/A100K	1		

Table 605-1 External Timebase Multiplier PCB Assembly —05 Option (Conclusion)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
C5, C6	Cap, ta, 10 μ F $\pm$ 20%, 15V	193623	56289	196D106X-0015KA1	REF		
L1, L2, L3	Inductor, bead, 6 turn	320911	89536	320911	3		
R1	Res, comp, 1.5K $\pm$ 5%, 1/4W	148031	01121	CB1525	1		
R2	Res, comp, 390 $\pm$ 5%, 1/4W	147975	01121	CB3915	1		
R3	Res, comp, 22K $\pm$ 5%, 1/4W	148130	01121	CB2235	1		
R4	Res, comp, 820 $\pm$ 5%, 1/4W	148015	01121	CB8215	1		
R5	Res, comp, 1K $\pm$ 5%, 1/4W	148023	01121	CB1025	1		
U1	IC, Dgtl, dual volt-controller multivibrator	320713	04713	MC4024P	1	1	
U2	IC, Dgtl, TTL, MSI decade counter	402545	01295	SN74LS90N	1	1	
U3	IC, TTL, phase-frequency detector	320721	04713	MC4044P	1	1	

Table 605-2. External Timebase Multiplier PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	EXTERNAL TIMEBASE MULTIPLIER PCB ASSEMBLY (EARLY) 1953A—05 Figure 605-4	455790	89536	455790	REF		
C601, C602	Cap, tant, 10 uF $\pm 20\%$, 15V	193623	56289	196D106X0015 JA1	1		
C603	Cap, cer, disc, 1 uF $\pm$ GMV 25V	369199	71590	UK-25-104	1		
C604	Cap, cer, disc, 27 pF $\pm 2\%$, 100V, mini npo	362749	80031	2222-631-10279	1		
CR601	Diode, switching lo p	203323	07919	1N4448	1		
L601	Inductor, bead, 6 turn	320911	89536	320911	1		
Q601	Xstr NPN Si, lo p	218396	01295	2N3904	1		
R601	Res, comp, 2.2k $\pm 5\%$, 1/4W	148049	01121	CB2225	1		
R602	Res, comp, 470 ohms $\pm 5\%$, 1/4W	147983	01121	CB4715	1		
R603, R605	Res, comp, 1k $\pm 5\%$, 1/4W	148023	01121	CB1025	2		
R604	Res, comp, 56k $\pm 5\%$, 1/4W	170738	01121	CB5635	1		
S601	Switch Slide, dpdt	407387	78488	SS-93	1		
U601	IC, Dgtl, TTL, dual volt-controlled multibrator	320713	04713	MC4024	1		
U602	IC, Dgtl, TTL, MSI, decade counters	293159	01295	SN7490N	1		
U603, U605	IC, Dgtl, TTL, pos NAND gates and inverters	292953	01295	SN7400N	2		
U604	IC, Dgtl, TTL, dual D-type edge-triggered flip-flops	310227	01295	SN7474N	1		
U606	IC, Dgtl, TTL, phase frequency detector	320721	04713	MC4044	1		
	Connector Jack	149112	74970	105-0753	2		
	Receptacle, conn.	375329	00779	85863-3	8		



Option —07 520 MHz Prescaler

607-1. Introduction

607-2. The channel C input, of the Model 1953A is intended for use with an optional frequency-prescaler. Option —07 is a prescaler which extends the operating range of the counter to 520 MHz. This prescaler has a frequency range extending from 50 MHz to 520 MHz with a specified sensitivity of 15 mV rms throughout the range. The option comprises a plug-in PCB assembly, a front-panel-mounted BNC connector, and the related components required both to adjust the power supply for correct operating voltages and to compensate the counter circuitry for the prescaling divisor. Option —07 must be ordered factory-installed in the 1953A, it is not field installable.

607-3. Theory of Operation

607-4. The main function of the prescaler is to reduce the frequency of the input signal to below 130 MHz for application to the main gate and decade counters. The prescaler also provides the necessary conditioning of the input signal to provide sufficient gain and the proper waveshaping. The frequency division factor for the prescaler is four.

607-5. As shown in Figure 607-1, the input signal is fed through an input protection fuse, F1, to the input of the first amplifier. Input limiting is provided by CR1 and CR2. The output of the second amplifier is applied to the input of a divider circuit which divides by a factor of four to reduce the input frequency to below 130 MHz. The prescaled signal, amplified by U1 and U2, divided and shaped by U3, is then fed to the main PCB assembly for application to the main gate and decade counters.

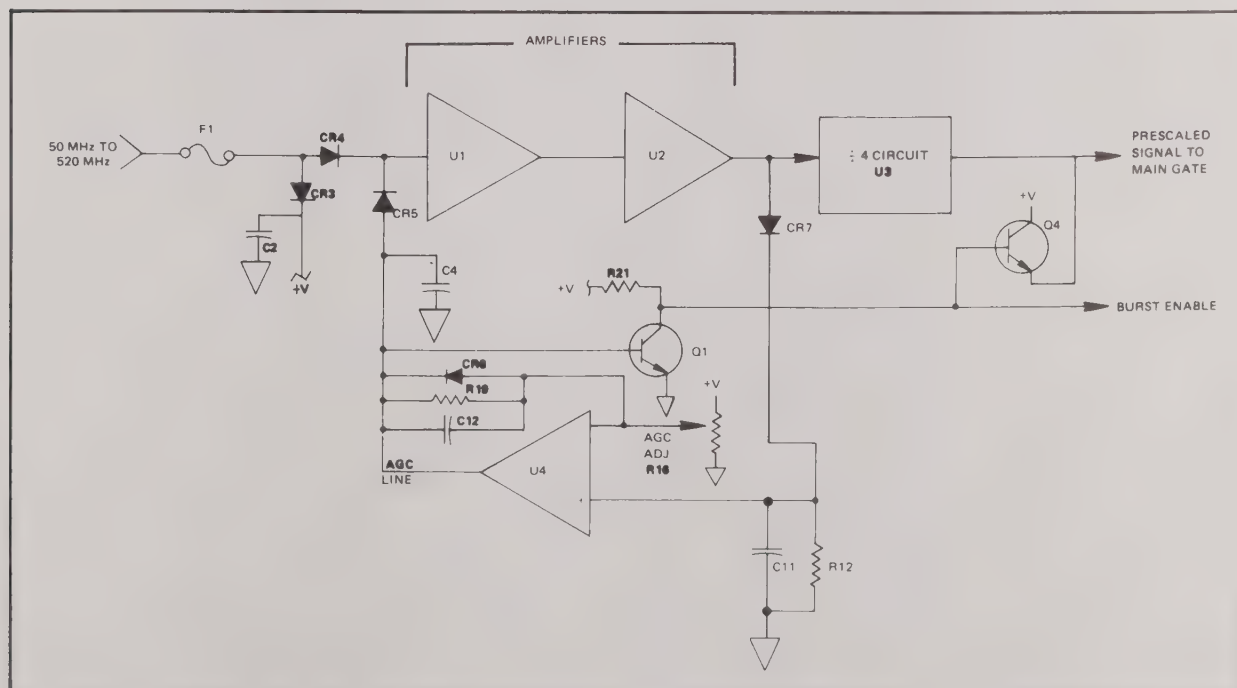


Figure 607-1. 520 MHz Prescaler, Block Diagram

607-6. The output of the second amplifier is also fed to an AGC circuit where it is rectified by CR7, filtered by C11/R12 and amplified by U4. The dc output of U4 is the AGC signal and controls the overall input signal level by means of CR5 and C4. Diode CR5 is a PIN-type diode whose impedance varies with the amount of bias applied. When AGC signal decreases due to a reduced input signal level the bias across CR5 is reduced causing an increase in impedance. This action results in a reduced shunting action of the input signal by CR5 and C4.

607-8. The AGC signal is also used to block the output of the prescaler when the input is below minimum acceptable amplitude. When this occurs, Q1 turns off and Q4 turns on to clamp the output to +5 volts.

607-9. Performance Checks

607-10. The performance check for the 520 MHz prescaler is actually a sensitivity check made at the upper and lower frequency limits. Proceed as follows:

- a. Connect a 1 GHz RF generator, terminated into 50 ohms, to a T-connector on the CHANNEL C input. Set the generator output for 50 MHz at approximately 15 mV rms.
- b. Connect the RF millivoltmeter (Refer to Table 4-1) to the %-connector on the input of the prescaler.
- c. Adjust the generator output for a reading of 15 mV rms on the RF millivoltmeter.
- d. Confirm that the counter reads 50 MHz $\pm$ generator accuracy.

- e. Change the generator output to 520 MHz and adjust the output for 15 mV rms on the RF millivoltmeter.
- f. Confirm that the counter reads 520 MHz $\pm$ generator accuracy.

607-11. Calibration

607-12. Calibration of the prescaler amounts to adjustment of the AGC level control located on the top edge of the prescaler PCB assembly. Proceed as follows:

- a. Remove the top dust cover from the instrument.
- b. Energize the counter and connect the RF generator to the CHANNEL C input connector. Select an output of 100 MHz at approximately 15 mV rms.
- c. On the counter, adjust the AGC control (R15) to a midpoint which produces a stable display.
- d. Reduce the input signal level until the display becomes unstable.
- e. Re-adjust the AGC control until the display is again stable.
- f. Repeat steps d and e until no additional sensitivity can be achieved.

607-13. List of Replaceable Parts

607-14. Table 607-1 is a list of replaceable parts for the 520 MHz Prescaler, Option -07. Refer to Section 5 for an explanation of the column entries. The component locations are illustrated in Figure 607-2.

Table 607-1. 520 MHz Prescaler Option -07 (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	520 MHz PRESCALER OPTION -07						
	520 MHz PRESCALER PCB ASSEMBLY	396291	89536	396291	1		
	Cable Assy (Front Panel to PCB)	406942	89536	406942	1		
	Following items are installed on the main PCB as part of the Prescaler Option -07.						
C91	Cap, elect, 470 uF -10/+100%, 40V	403030	99392	39CS50FJ52	1	1	
U13	IC, TTL, 4-bit binary counter	320739	01295	SN7493N	1		
U91	Diode Bridge	296509	09423	FB200	1		
U93	IC, linear, vol reg	429225	07263	F7818UC	1	1	
	520 MHz PRESCALER PCB ASSEMBLY Figure 607-2.	396291	89536	396291	REF		
C1, C2, C4, C6, C7, C9,	Cap, cer, .001 uF $\pm 20\%$, 100V	402966	72982	8121-A100-W5R 102M	6		
C8	Cap, cer, 22 pF $\pm 20\%$, 500V	369157	72982	831-000-C060-220	1		
C3, C11, C12	Cap, cer, 1000 pF $\pm 10\%$, 500V	357806	71590	CF102	3		
C5, C10	Cap, cer, 0.01 uF $\pm 20\%$, 100V	407361	72982	8121-A100-W5R-103M	2		
C13, C14	Cap, cer, 0.01 uF $\pm 20\%$, 100V	149153	56289	C023B101F103M	2		
CR3, CR4, CR5	Diode, small signal	402776	28480	HP5082-3379	3		
CR6, CR7	Diode, hot carrier	369595	07263	FH1100	4		
CR8	Diode, switching, lo p Si	203323	07919	1N4448	1		
CR9	Diode, zener	159798	07263	1N751A	1		
F1, F2	Fuse, .2 amp, 2.6 ohm, maxcold	370557	75915	273200	2		
J5	Connector, test jack	149112	74970	105-0753	2		
	Amp Receptacle	375329	00779	85863-3	5		
J20	Connector, coaxial, snap-on, pcb mount right angle, con-hex type	353243	98291	51-053-000	1		
Q1, Q3	Xstr, NPN Si	177105	07263	2N3565	2		

Table 607-1. 520 MHz Prescaler PCB Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
Q2	Xstr, sm sig, PNP, Si, To -92	352369	07263	2N4403	1	1	
Q4	Xstr, NPN, Si, lo p	369645	07263	2N4274	1		
R1, R14	Res, comp, 82 ohms $\pm 5\%$, 1/4W	149484	01121	CB8205	2		
R2	Res, comp, 22 ohms $\pm 5\%$, 1/4W	147884	01121	CB2205	1		
R3, R5, R11	Res, comp, 470 ohms $\pm 5\%$, 1/4W	147983	01121	CB4715	3		
R4	Res, comp, 680 ohms $\pm 5\%$, 1/4W	148007	01121	CB6815	1		
R6, R17, R21	Res, comp, 1k $\pm 5\%$, 1/4W	148023	01121	CB1025	3		
R7, R10, R12, R13	Res, comp, 2.7k $\pm 5\%$, 1/4W	170720	01121	CB2725	4		
R8	Res, comp, 68 $\pm 5\%$, 1/4W	147918	01121	CB6805	1		
R9, R15, R20	Res, 10k $\pm 5\%$, 1/4W	148106	01121	CB1035	3		
R16	Res, var, comp, 10k $\pm 20\%$, 20W	385393	54869	PT10(25)10K	1	1	
R18	Res, comp, 2.2M $\pm 5\%$, 1/4W	198390	01121	CB2255	1		
R19	Res, comp, 330k $\pm 5\%$, 1/4W	192948	01121	CB3345	1		
U1	I.C. Linear, VHF/UHF, wide band amplifier	392977	35784	OM185	1	1	
U2	I.C. Linear, thin film, hybrid, amplifier 5 - 400 MHz	402594	24539	GPD402	1	1	
U3	I.C. Digital ECL, divide by 4 counter	402719	07263	F11C05PC	1	1	
U4	I.C. Op Amp mini dip	402750	07263	741TC	1	1	
XF1, XF2	Fuse Socket, spring type	403642	00779	50863-8	4		
XU3	Socket, IC, 14 pin	291542	00779	583527	1		

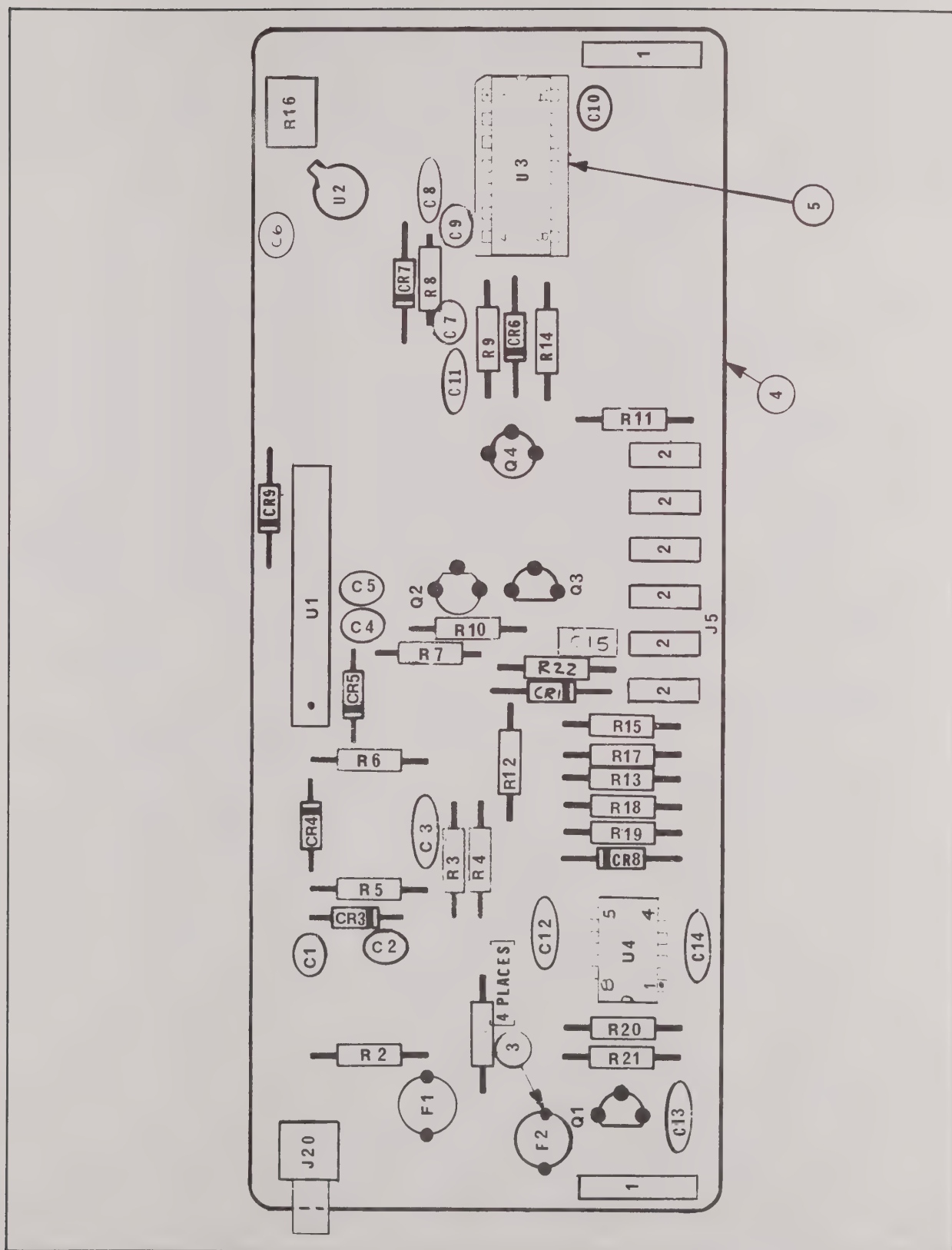


Figure 607-2. 520 MHz Prescaler, PCB Assembly

Option —10 Ovenized Oscillator

610-1. Introduction

610-2. The Option —10 Ovenized Oscillator affords a higher degree of timebase stability to the Model 1953A than either of the TCXO's available. The specifications for Option —10 are given in Section 1. The unit is installed on the inside of the rear panel of the 1953A, and requires re-arrangement of the instrument's power switching. A switch installed on the rear panel of the 1953A is used to activate the heaters independently of the power switch for the instrument itself. The option must be ordered factory-installed in the 1953A when the instrument is purchased, it is not field installable.

610-3. Calibration

610-4. Calibration of the Ovenized Oscillator is similar to that of the other timebases. Proceed as follows:

- a. Connect 1953A to ac line power.
- b. Turn CYCLE RATE control cw, off the OFF detent.
- c. Set FUNCTION switch to FREQ A.
- d. Set CONT/TRIG switch to TRIG.
- e. Connect 10 MHz frequency standard to CHANNEL A connector.
- f. Adjust channel A TRIGGER LEVEL control to establish proper input signal triggering.
- g. Set RANGE switch to 10s (GATE 4).
- h. Momentarily press RESET button. After 10 seconds 1953A display should indicate: 10000.0000 kHz.
- i. If display is incorrect locate the adjustment screw access hole on the rear panel. Using an insulated tuning tool, turn the adjustment slightly.
- j. Momentarily press RESET button. Observe the display for a change in the readout.
- k. Repeat steps h, i and j until the display reads 10000.0000 kHz.

Table 610-1. Oven-Stabilized Timebase, Option -10

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	OVEN-STABILIZED TIMEBASE Option -10 <i>NOTE</i> <i>Unless otherwise noted components are installed on the main pcb. Refer to figure 5-6.</i>						
C91	Cap, elect, 4000 uF -10/+100%, 25V	370742	99392	39C25JJ43	1	1	
C121	Cap, cer, 10,000 pF $\pm 20\%$, 100V	407361	72982	8121-A100-W5R-103M	1		
C122, C123	Cap, tant, 10 uF $\pm 20\%$, 35V	417683	56289	196D106X0035 PE4	2		
R121	Res, var, cer, 10k $\pm 20\%$, 1/2W	267880	11236	190PC103B	1	1	
R128	Res, comp, 1k $\pm 5\%$, 1/4W	148023	01121	CB1025	1		
R129	Res, comp, 10k $\pm 5\%$, 1/4W	148106	01121	CB1035	1		
S121	Switch, toggle 	327734	09353	7201LHPZG1	1		
U7	Oscillator 	441170	12020	73-43	1		
U91	Rect, bridge	296509	09423	FB200	1		
U101	Reg assy + 18V	443713	89536	443713	1		
	Cable Assy	443705	89536	443705	1		
	Decal 	428052	89536	428052	1		
	 Attached to rear panel						
	 Attached to inside right chassis of instrument.						
	 Attached to front panel-power switch.						

Option —11 Basic Remote Control Unit

611-1. Introduction

611-2. Option —11 is a remote control unit allowing remote operation of the 1953A. Option —11 is the Basic Remote Control Unit, permitting control of the essential functions required for remote operation of the 1953A.

611-3. Basic Remote Control Unit

611-4. Option —11 is the basic remote programming option. It consists of a single PCB and a ribbon-cable assembly. When installed it allows the 1953A to be operated from a remote station. The option allows full Range and Function selection; control of the trigger edge selectors Slope A and Slope B, and a "Front panel lockout" command (low true) which disables the manual front panel controls corresponding to these functions and places the functions under remote control. In addition, this option provides for remote analog control of the channel A and B trigger levels. When under remote control the 1953A always operates in a single - shot mode, and the Cycle Rate and CONT/TRIG controls are disabled. All inputs are TTL compatible, low true commands that can also be controlled by contact-closure to ground.

611-5. Installation

611-6. Remote control Option —11 can be installed at the factory upon request when ordering the 1953A, it is not field installable.

611-7. Operation

611-8. The following lists and Table 611-1 give the relevant data for operating the 1953A in the Basic Remote Control mode.

a.	Function (One line of 7 to be low)		
	FREQ A	(A)	fan-in = 1
	FREQ C	(C)	fan-in = 1
	FREQ A/B	(A/B)	fan-in = 1
	PERIOD A	(PA)	fan-in = 1
	TIME INTERVAL	(TI)	fan-in = 1

A GTD BY B	(A x B)	fan-in = 1
CHECK	(CH)	fan-in = 1

- b. Range (one line of 6 to be low)
- | | | | | |
|-------|-----------------|-------|-----|------------|
| 0.1ms | 10 ⁰ | 0.1us | (1) | Fan-in = 1 |
| 1ms | 10 ¹ | 1us | (2) | Fan-in = 1 |
| 10ms | 10 ² | 10us | (3) | Fan-in = 1 |
| 0.1s | 10 ³ | 0.1ms | (4) | Fan-in = 1 |
| 1s | 10 ⁴ | 1ms | (5) | Fan-in = 1 |
| 10s | 10 ⁵ | 10ms | (6) | Fan-in = 1 |
- c. Slope (one line per channel)
Slope A (EXT SA) low = positive Fan-in = 3
Slope B (EXT SB) low = positive Fan-in = 1
- d. Reset (one line, low true)
When the reset line is brought low and released, new measurement sequence will start without resetting the display.
Note: This same line is used on DOU option.
- e. The following outputs are provided:
1. Power Sense (SP) high = on
A+5 Volt level indicates that the instrument is on
 2. Overflow Status (OVFL) high true
Outputs a high level when an overflow condition exists.
 3. System Ready low true
Signals the completion of a measurement cycle. (Note that the System Ready appears about 3ms before the DOU ready)
 4. Channels A and B signal outputs (SMA; SMB) TTL.
These are not normally connected, except by special request. To connect these outputs, jumper both W5 and W6 on the main PCB.

CAUTION!

These outputs should be connected only in applications where the maximum channel A or B count frequency is below 25 MHz. Exposed wiring external to the unit should be kept to a minimum to prevent signal feedback.

- f. Also provided are two Analog Trigger Level input/outputs (ATL-A and ATL-B) which can be used for measuring the internally-generated trigger levels with an external voltmeter, or for defining the trigger levels from an external dc source. The input impedance is 20K, and the response time is 2 ms. Usable range is ± 1 volt, and the maximum safe level is ± 5 volts. Operation with X10 attenuation extends the apparent range to ± 10 V.
- g. Although the counter will operate in a single-shot mode when under remote control, automatic measurement cycling can be established by connecting the System Ready output into the Reset input. The cycle rate will be the maximum attainable with

the instrument and will be equal to the gate time plus the conversion time (50 μ s).

611-9. External Connections

611-10. The input commands needed to operate the Remote Control Unit are provided in Table 611-1. The pin numbers identified in the table correspond to the pin numbers on the 50 pin connector supplied with the option.

611-11. List of Replaceable Parts

611-12. Table 611-2 is a list of replaceable parts for the Remote Control Unit, Option -11. Refer to Section 5 for an explanation of the column entries. The component locations are illustrated in Figure 611-1.

Table 611-1. RCU Connections To External Equipment

Pin	Signal	Low Logic Equals	High Logic Equals	Fan In
B	ATL A	Analog Trigger Level A Input Trigger Level Monitor Output Analog Trigger Level B Input Trigger Level Monitor Output		
C	ATL B			
P	$\overline{\text{SA}}$	+ Slope	– Slope	1
R	SYSTEM READY	System Ready	System Not Ready	
U	PA	Period A Function		1
V	$\overline{4}$	0.1s Range		1
W	$\overline{2}$	1.0 ms Range		1
X	$\overline{\text{AXB}}$	A GTD by B Function		1
Y	$\overline{\text{CH}}$	Self check Function		1
Z	$\overline{6}$	10s Range		1
a	OVFL		Overflow Output	
b	$\overline{\text{A}}$	FREQ A Function		1
c	$\overline{\text{SR}}$	Sense Remote		
3	SP		Positive (Down on)	
12	$\overline{\text{SMA}}$	TTL Output Equal to CHL-A Input	Not Normally	
13	SMB	TTL Output Equal to CHL-B Input	Connected	
14	$\overline{\text{SB}}$	+ Slope	– Slope	1
17	$\overline{\text{C}}$	FREQ C Function		1
18	$\overline{\text{TI}}$	T.I. A-B Function		1
19	1	0.1 ms Range		1
20	Remote $\overline{\text{EXT}}$	Front Panel Lockout		5
21	$\overline{\text{A/B}}$	FREQ A/B Function		1
22	$\overline{5}$	1.0s Range		1
23	$\overline{\text{EXT-}}$ $\overline{\text{RESET}}$	Resets Counter		
24	$\overline{3}$	10 ms Range		1
25	Ground			

NOTES ON RCU CONNECTIONS TABLE

TTL fan-ins are given where relevant. The remaining inputs are CMOS compatible with internal 100K ohm pull-up to +5 volts.

Table 611-2. Basic Remote Control Unit

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
S121 	BASIC REMOTE CONTROL UNIT OPTION 11						
	<i>NOTE: Contains additional items for the Model 1953A Final Assembly.</i>						
	Basic RCU PCB Assy	405563	89536	405563	1		
	Cover, optional 	398016	89536	398016	1		
	Connector Kit	410241	89536	410241	1		
	Remote Decal	408617	89536	408617	1		
	Switch, toggle, dpdt (installed on rear panel) Replaces cover, basic P/N 398024	327734	09353	7201LHPZGI	1	1	

Table 611-3. Basic RCU PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	BASIC RCU PCB ASSEMBLY Figure 611-1.	405563	89536	405563	REF		
C711	Cap, Ta, 10 uF $\pm 20\%$, 15V	193623	56289	196D106X0015 KA4	1		
C712	Cap, cer, 0.002 uF $\pm$ GMV, 1 kV	105569	71590	DA140-139CB	1		
CR702 CR703, CR704, CR705	Diode, switching low, power, Si	203323	07919	1N4448	4	1	
J81, J82	Flat Cable Assembly	393520	08261	5142-006	2		
R751, R763	Res, comp, 100 ohms $\pm 5\%$, 1/4W	147926	01121	CB1015	1		
R752, R753	Res, comp, 82 ohms $\pm 5\%$, 1/4W	149484	01121	CB8205	2		
R758	Res, comp, 390 $\pm 5\%$, 1/4W	147975	01121	CB3915	1		
R759, R760, R762	Res, comp, 4.7k $\pm 5\%$, 1/4W	148072	01121	CB4725	3		
U711, U712, U713	IC, TTL, tri-state, hex buffer	408146	07263	CM8095N	3	1	

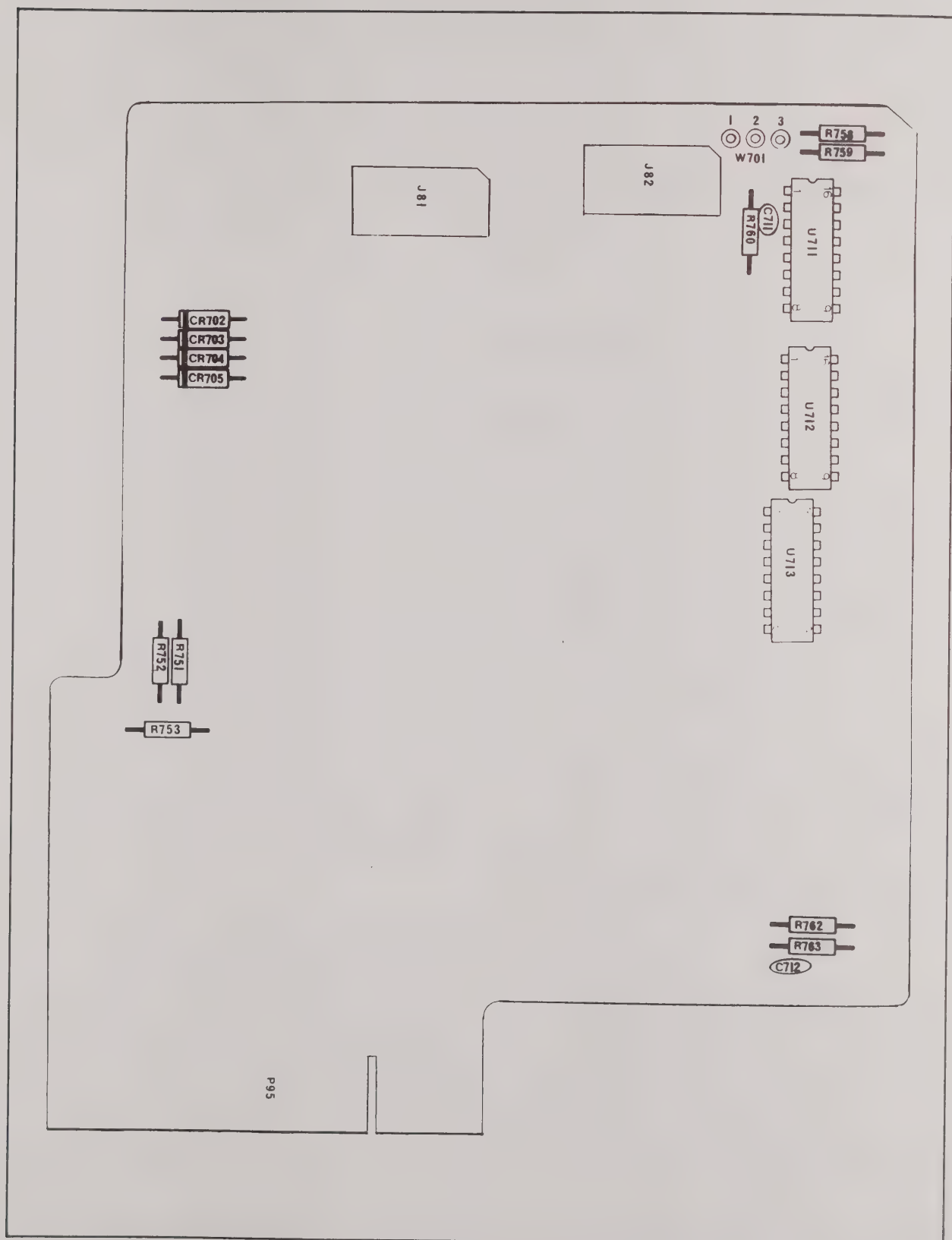


Figure 611-1. RCU Basic PCB Assembly

Option —12 Remote Control Unit

612-1. Introduction

612-2. Option —12 is a remote control unit allowing remote operation of the 1953A. Option —12 is the Full Remote Control Unit, comprising the same features as the —11 Option, but including, in addition, the remaining functions necessary for complete remote digital control of the 1953A.

612-3. Full Remote Control Unit

612-4. Option —12 includes all of the programming features of Option —11 plus remote control of the AC/DC coupling, attenuation selectors, separate/common input status between channels A and B, and the trigger levels of channel A and B. The Basic configuration allows full range and function selection, control of trigger edge selectors Slope A and Slope B, and a “Front Panel Lockout” command to disable the manual front panel controls corresponding to those functions to place them under exclusive remote control. Under remote control, the 1953A operates in a single-shot mode and the Cycle Rate and CONT/TRIG controls are disabled.

612-5. Two internal D/A converters are used for programming the trigger levels over a –1 to +1 volt range in 10 mV steps. A separate local trigger disable allows control of the local trigger under remote control operations. Two BCD digits, plus a sign, are provided for each channel (A and B). All analog function switches are operated by means of relays working from TTL or contact level closures. No inputs should be forced low when the system is used in the local operating mode.

612-6. Installation

612-7. Option —12 requires installation at the factory. The option includes three PCB assemblies, RCU 1, RCU2 and RCU 3.

612-8. Operation

612-9. The following lists and Table 612-1 give the relevant data for operating the 1953A in the Full Remote Control mode.

- a. Function (One line of 7 to be low)

FREQ A	(A)	fan-in = 1
FREQ C	(C)	fan-in = 1
FREQ A/B	(A/B)	fan-in = 1
PERIOD A	(PA)	fan-in = 1
TIME INTERVAL	(TI)	fan-in = 1
A GTD BY B	(A x B)	fan-in = 1
CHECK	(CH)	fan-in = 1
- b. Range (One line of 6 to be low)

0.1ms	10 ⁰	0.1us	(1)	Fan-in = 1
1ms	10 ¹	1us	(2)	Fan-in = 1
10ms	10 ²	10us	(3)	Fan-in = 1
0.1s	10 ³	0.1ms	(4)	Fan-in = 1
1s	10 ⁴	1ms	(5)	Fan-in = 1
10s	10 ⁵	10ms	(6)	Fan-in = 1
- c. Slope (One line per channel)

Slope A (EXT SA) low = positive	Fan-in = 3
Slope B (EXT SB) low = positive	Fan-in = 1
- d. D/A Converters:

Resolution	= 1%
Accuracy	= +5% of setting +2 mV
Temperature Stability	= 200 uV/°C
All inputs are high true	
The x10 attenuator extends the apparent range to ±10V in 100 mV steps.	
- e. AC/DC Coupling (1 line per channel)

Channel A (DA) low = AC Coupling	Fan-in = 1
Channel B (DB) low = AC Coupling	Fan-in = 1
- f. Attenuator (1 line per channel)

Channel A (TA) low = x1	Fan-in = 1
Channel B (TB) low = x1	Fan-in = 1

Table 612-1. RCU Connections To External Equipment (Continued)

Pin	Signal	Low Logic Equals	High Logic Equals	Fan in
A	Sign A	Negative	Positive	
B	ATL A	Analog Trigger Level A Input Trigger Level Monitor Output Analog Trigger Level B Input Trigger Level Monitor Output		
C	ATL B			
D	A "1"			TRUE
E	A "4"		TRUE	
F	A "10"		TRUE	
H	A "40"		TRUE	
J	B "1"		TRUE	
K	B "4"		TRUE	
L	B "10"		TRUE	
M	B "40"		TRUE	
N	$\overline{SC}$	A, B Inputs SEP	A, B Inputs COM	1
P	$\overline{SA}$	+ Slope	— Slope	1
R	SYSTEM READY	System Ready	System Not Ready	
S	$\overline{DB}$	CH-B AC Coupled	CH-B DC Coupled	1
T	$\overline{DA}$	CH-A AC Coupled	CH-A DC Coupled	1
U	$\overline{PA}$	Period A Function		1
V	$\overline{4}$	0.1s Range		1
W	$\overline{2}$	1.0ms Range		1
X	$\overline{AXB}$	A GTD by B Function		1
Y	$\overline{CH}$	Self Check Function		1
Z	$\overline{6}$	10s Range		1
a	OVFL		Overflow Output	
b	$\overline{A}$	FREQ A Function		1
c	$\overline{SR}$	Sense Remote		
1	$\overline{EXT-T}$	Local Trigger Disable	Local Trigger Enable	
2	Sign-B	Negative	Positive	
3	SP		Positive (Down on)	
4	A "2"		TRUE	
5	A "8"		TRUE	
6	A "20"		TRUE	
7	A "80"		TRUE	
8	B "2"		TRUE	
9	B "8"		TRUE	
10	B "20"		TRUE	
11	B "80"		TRUE	
12	$\overline{SMA}$	TTL Output Equal to CHL-A Input	Not Normally	
13	$\overline{SMB}$	TTL Output Equal to CHL-B Input	Connected	
14	$\overline{SB}$	+ Slope	— Slope	1
15	$\overline{TB}$	CH-B Atten x1	CH-B Atten x10	1
16	$\overline{TA}$	CH-A Atten x1	CH-A Atten x10	1
17	$\overline{C}$	FREQ C Function		1

Table 612-1. RCU Connections To External Equipment (Concluded)

Pin	Signal	Low Logic Equals	High Logic Equals	Fan in
18	$\overline{TI}$	T.I. A-B Function		1
19	1	0.1 ms Range		1
20	$\overline{EXT}$	Front Panel Lockout		5
21	$\overline{A/B}$	FREQ A/B Function		1
22	5	1.0 s Range		1
23	$\overline{EXT-RESET}$	Reset Counter		
24	3	10 ms Range		1
25	Ground			

NOTES ON RCU CONNECTIONS TABLE

- (1) Pins D through M and 4 through 11, as per the table, represent the binary coded decimal inputs for the trigger level controls of channels A and B. The trigger level is divided into 10 mV steps, requiring two sets of binary coded decades, one for units and one for tens. The trigger level signs are provided by pins A and 2. Pins B and C, named ATL-A and ATL-B respectively, can be used as either analog inputs for an externally applied dc trigger level, or as output terminals for external measurement of the trigger level when that level stems from either the D/A converter or the front panel trigger level adjustments.
- (2) TTL fan-ins are given where relevant. The remaining inputs are CMOS compatible with internal 100K ohm pull-up to +5 volts.

- g. Separate/Common (1 line)
(SC) low = separate Fan-in = 1

- h. The two Analog Trigger Level lines are also provided for checking the operation of the internal D/A's or analog programming the trigger levels whenever the D/A's are disabled.

- i. Reset (one line, low true)
When the reset line is brought low and released, a new measurement sequence will start without resetting the display.
Note: This same line is used on DOU option.

- j. The following outputs are provided:
1. Power Sense (SP) high = on
A +5 Volt level indicates that the instrument is on
 2. Overflow Status (OVFL) high true
Outputs a high level when an overflow condition exists.
 3. SYSTEM READY low true
Signals the completion of a measurement cycle. (Note that the System Ready appears about 3 ms before the DOU ready)
 4. Channels A and B signal outputs (SMA; SMB) TTL.
These are not normally connected, except by special request. To connect these outputs, jumper both W5 and W6 on the main PCB.

CAUTION!

These outputs should be connected only in applications where the maximum channel A or B count frequency is below 25 MHz. Exposed wiring external to the unit should be kept to a minimum to prevent signal feedback.

- k. Also provided are two Analog Trigger Level input/outputs (ATL-A and ATL-B) which can be used for measuring the internally-generated trigger levels with an external voltmeter, or for defining the trigger levels from an external dc source. The input impedance is 20K, and the response time is 2 ms. Usable range is ± 1 volt, and the maximum safe level is ± 5 volts. Operation with X10 attenuation extends the apparent range to $\pm 10V$.

- l. Although the counter will operate in a single-shot mode when under remote control, automatic measurement cycling can be established by connecting the System Ready output into the Reset input. The cycle rate will be the maximum attainable with the instrument and will be equal to the gate time plus the conversion time (50 us).

- m. Whenever Option 12 is installed, the overall 1953A specifications are changed in two areas:
1. Input capacity increases to 45 pF max.
 2. Overload capability becomes:
DC + Peak AC must not exceed 250 volts, when

in steady state condition, this decreases to 100 volts maximum whenever any of the following lines are switched:

DA	Channel A coupling
DB	Channel B coupling
TA	Attenuation, Channel A
TB	Attenuation, Channel B
SC	Separate/Common

612-10.External Connections

612-11. The input commands needed to operate the Remote Control Unit are provided in Table 612-1. The pin numbers identified in the table correspond to the pin numbers on the 50 pin connector supplied with the option.

612-12.Theory of Operation of the Digital to Analog Converter

612-13. The Full Remote Control Unit, Option -12, provides the remote operating station with the ability to digitally program the trigger level. Figure 612-1 is a basic illustration of the remote trigger level control circuit.

612-14. The digital inputs for channel A and channel B are applied to two Digital to Analog Converters each containing

current sourcing amplifiers connected to resistors of selected value. The resistor values are selected to provide a trigger level output, in 10mV steps, up to ± 1 volt in the x1 ATTEN setting. When the x10 ATTEN setting is selected the trigger level output is in 100 mV steps up to ± 10 volts.

612-15. For both channels A and B the SIGN input controls switching FET's that select either a positive output or a negative output for the trigger level control. The external trigger level control is enabled by a LOW input to the EXT-T pin on the RCU rear panel connector.

612-16.Calibration Procedure for Digital Trigger Level Control

612-17. The calibration requires use of a DVM. See Table 4-1 for recommended type. Make reference to Table 612-1 as necessary for pin designations on P95, and to reference designator Figure 612-4 (RCU 3 PCB Assembly) for location of trimpots R701, R704, R705, R708.

612-18. Calibrate Digital Trigger Level Controls of Channels A and B as follows:

- Connect 1953A to line power.
- Rotate Cycle-Rate control cw, off the OFF detent.

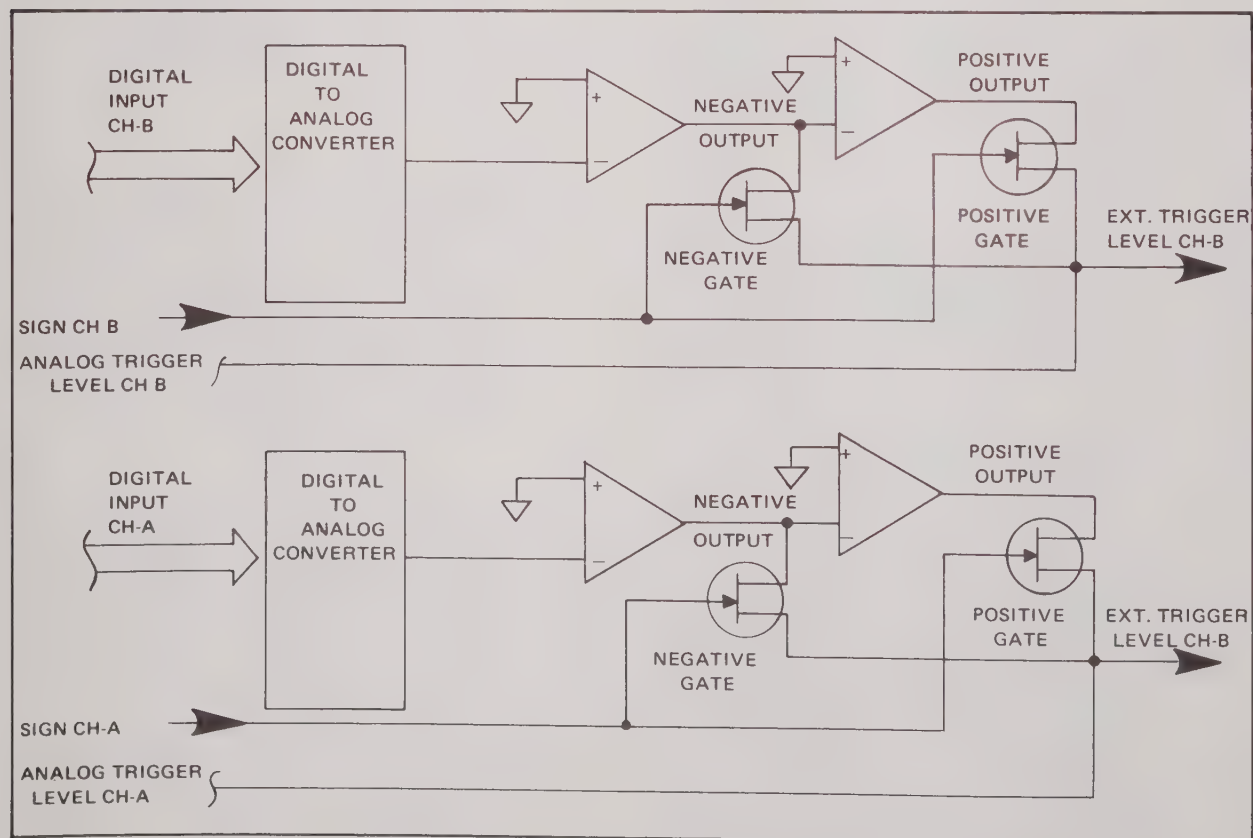


Figure 612-1. Trigger Level Control, Block Diagram

- c.

Channel A calibration

1. Connect EXT-T to ground. This enables the digital trigger.

2. Connect Digital Input pins (D, E, F, H, 4, 5, 6, 7) of Channel A to ground (O state).

3. Connect DVM to pin B (ATL-A) of P95 (RCU input).

4. Set SIGN-A to negative (ground pin A).

5. Adjust trimpot R708 until DVM reads zero ± 0.1 mV.

6. Set SIGN-A to positive (open pin A).

7. Adjust trimpot R705 until DVM reads zero ± 0.1 mV.
2. Connect the Digital Input pins (J, K, L, M, 8, 9, 10, 11) of Channel B to ground (O state).

3. Connect the DVM to pin C (ATL-B) of P95 input).

4. Set SIGN-B to negative (ground pin 2).

5. Adjust trimpot R704 until the DVM reads zero ± 0.1 mV.

6. Set SIGN-B to positive (open pin 2).

7. Adjust R701 until the DVM reads zero ± 0.1 mV

612-19. List of Replaceable Parts

612-20. Tables 612-2, 612-3 and 612-4 are lists of replaceable parts for the full remote control unit. Refer to Section 5 for an explanation of the column entries. The component locations for RCU1, RCU2 and RCU3 PCB's are illustrated in Figures 612-2, 612-3 and 612-4 respectively.

Table 612-2. Remote Control Unit

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
S121	REMOTE CONTROL UNIT Option -12						
	NOTE: Contains additional items for the Model 1953A Final Assembly						
	RCU 1 PCB Assy 	396242	89536	396242	1		
	RCU 2 PCB Assy 	396259	89536	396259	1		
	RCU 3 PCB Assy	396150	89536	396150	1		
	Decal, remote	408617	89536	408617	1		
	Cover Optional 	398016	89536	398016	1		
	Connector Kit	410241	89536	410241	1		
	Switch, toggle dpdt (Installed on Rear Panel)	327734	09353	7201LPZGI	1	1	
	 Replace Input PCB Assy A4 P/N 396127						
	 Replaces Cover, Basic P/N 398024						

Table 612-3. RCU 1 PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	RCU 1 PCB ASSEMBLY						
	Option -12 Figure 612-2	396242	89536	396242	REF		
DS401 thru DS404	LED	385898	28480	5082-4487	4	1	
J1	Connector, blk, PCB test	149112	74970	105-0753	2		
	Receptacle	375329	00779	85863-3	12		
P10	Connector Post Uninsulated	376574	00779	5166-333-68	7		
R410 thru R413	Res, comp, 47 $\pm 5\%$, 1/4W	147892	01121	CB4705	4		
S108 thru S114	Slide Sw, spdt	380113	79727	GF-124-SPDT	7	2	
U401	Res, Ntwk. -7 10K $\pm 5\%$, 1.5W	364000	71450	760-1	1	1	
U402	I.C. TTL, hex inc. open coll	379305	01295	SN7405N	1	1	

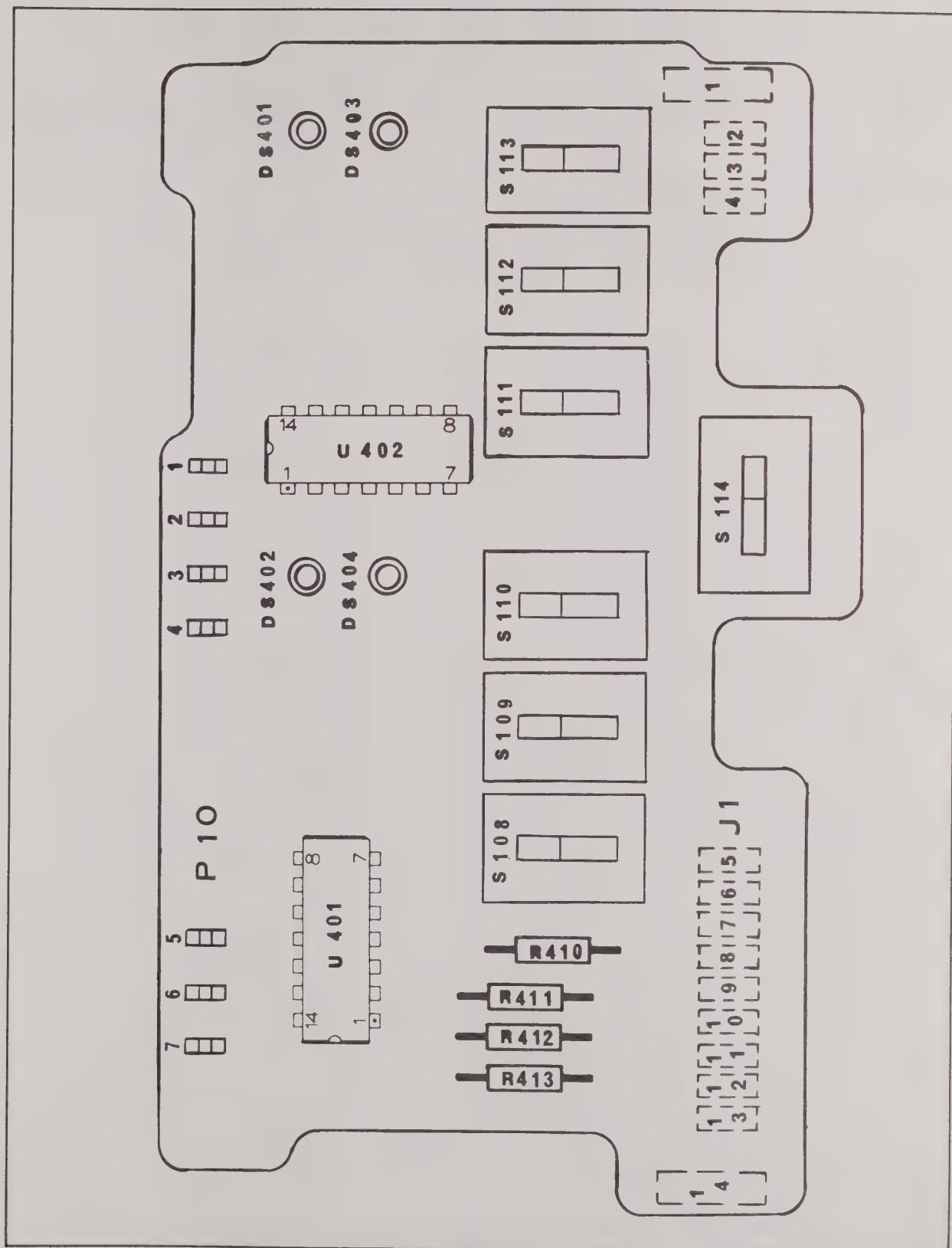


Figure 612-2. RCU 1 PCB Assembly

Table 612-4. RCU 2 PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	RCU 2 PCB ASSEMBLY Option -12 Figure 612-3	396259	89536	396259	REF		
A404 thru A411	Relay, dry reed monostable, spst, 65 mW 380 ohms, 10%	334920	24211	GB-831A-4E	8		
C401, C402	Cap, mylar 0.1 uF $\pm 10\%$, 250V	161992	73445	C280AE/N00K	2		
C403 C404	Cap, cer, 1.5 pF ± 0.25 pF, 1 kV	178475	56289	10TCCV15-NPO	2		
J2	Conn Test Jack, Blk.	149112	74970	105-0753	2		
	Receptacle	375329	00779	85863-3	9		
R401, R402	Res, comp, 910K $\pm 5\%$, 1/4W	285338	01121	CB9145	2		
R403, R404	Res, comp, 100K $\pm 5\%$, 1/4W	148189	01121	CB1045	2		
R405, R406	Res, var, 10K 1/2W $\pm 30\%$	385880	89536	385880	2		
U403	I.C. TTL, hex inv, open coll	379305	01295	SN7405N	1	1	

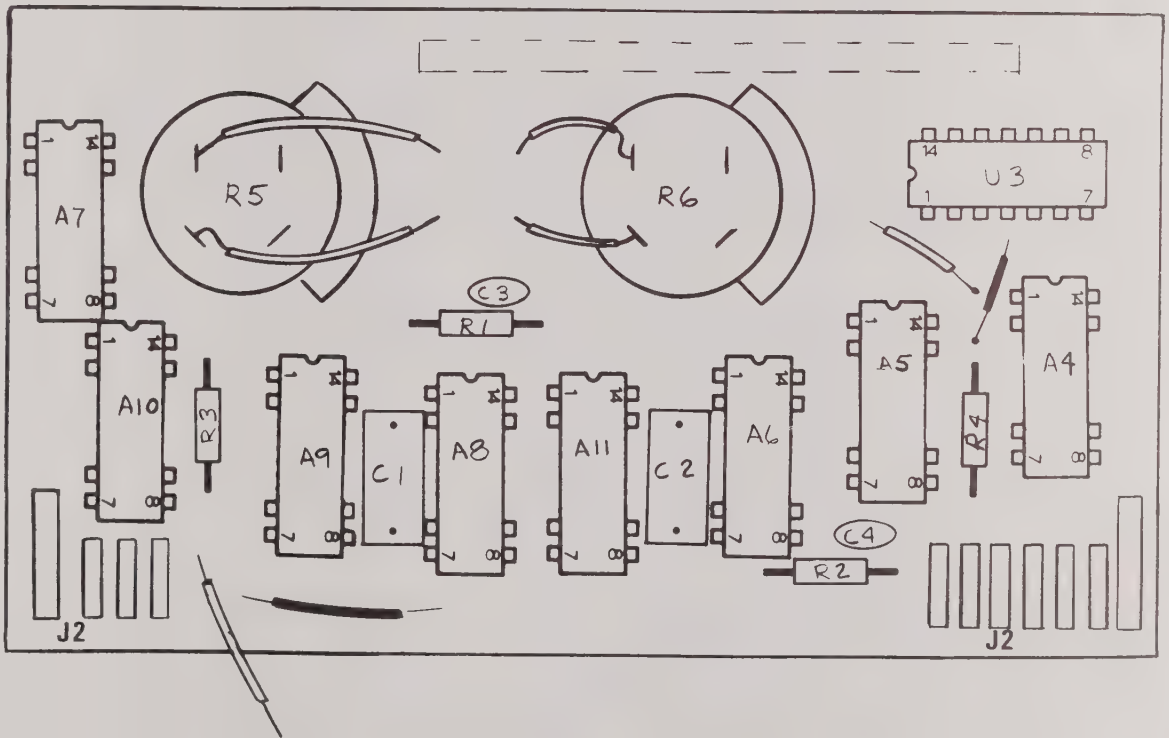


Figure 612-3. RCU 2 PCB Assembly

Table 612-5. RCU 3 PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	RCU 3 PCB ASSEMBLY						
	Option -12 Figure 612-4	396150	89536	396150	REF		
C701, C705, C711	Cap, tant, 10 uF, 20%, 15V	193623	56289	196D106X0015-5KA4	3		
C702, C704, C706, C709	Cap, cer disc, 100 pF $\pm 10\%$, 50 VDCW	105593	71590	DD101	4		
C703, C708	Cap, cer, disc, 0.1 uF $\pm 20\%$, 50 VDC W	149146	56289	33C41B6	2		
C712	Cap, cer, 0.002 uF $\pm$ GMV, 1 kV	105569	56289	DA140-139CB	1		
CR701, CR706, CR707	Diode, zener, 400 mW, 12V	110726	07910	1N946B	3	1	
CR702, CR703, CR704, CR705	Diode, Si, hi speed, 75V, 150 mA	203323	07919	1N444B	4	1	
J81, J82	Flat Cable Assy	393520	08261	5142-006	2		
Q701 thru Q704	Xstr, FET, N-channel, Si, hi speed	404277	01295	TIS73	4		
R701, R704, R705, R708	Res, Trimpot, 10K, 10V, horiz mount	369553	54869	PT10V-10K	4		
R702, R703, R706, R707	Res, comp, 2.2M $\pm 5\%$, 1/4W	198390	01121	CB2255	4		
R709, R747	Res, MF, 95.3K $\pm 0.1\%$, 1/8W	346858	91637	MFF1-89532B	2		
R710, R743	Res, MF, 4.32K $\pm 1\%$, 1/8W	294819	91637	MFF1-84321F	2		
R711, R741	Res, MF, 47.5K $\pm 0.1\%$, 1/8W	344523	91637	MFF1-84752B	2		
R712, R742	Res, MF, 2.32K $\pm 1\%$, 1/8W	260315	91637	MFF1-82321F	2		

Table 612-5. RCU 3 PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R713, R714, R719, R726	Res, MF, 10K $\pm 0.1\%$, 1/8W	343459	91637	MFF1-81002B	4		
R715, R716, R727, R728	Res, comp, 27K $\pm 5\%$, 1/4W	148148	01121	CB2735	4		
R717, R729	Res, comp, 10K $\pm 5\%$, 1/4W	184106	01121	CB1035	2		
R718, R730, R731, R759 thru R762	Res, comp, 4.7K $\pm 5\%$, 1/4W	148072	01121	CB4725	7		
R720, R732, R733	Res, comp, 47K $\pm 5\%$, 1/4W	148163	01121	CB4735	3		
R721, R734	Res, MF 8.06K $\pm 1\%$, 1/8W	294942	91637	MFF1-8061F	2		
R722, R723, R724, R725	Res, comp, 1k $\pm 5\%$, 1/4W	148023	01121	CB1025	4		
R735, R745	Res, MF 402K $\pm 1\%$, 1/8W	348391	91637	MFF1-84023F	2		
R736, R746	Res, MF 200 K $\pm 1\%$, 1/8W	261701	91637	MFF1-82003F	2		
R737, R748	Res, MF 1M, $\pm 1\%$, 1/8W	269797	91637	MFF1-81004F	2		
R738, R744	Res, MF 499K $\pm 1\%$, 1/8W	349191	91637	MFF1-84993F	2		
R739, R749	Res, comp, 2M $\pm 5\%$, 1/4W	268771	01121	CB2055	2		
R740, R750	Res, comp, 3.9M $\pm 5\%$, 1/4W	188417	01121	CB3955	2		
R751, R763	Res, comp, 100 $\pm 5\%$, 1/4W	147926	01121	CB1015	2		

Table 612-5. RCU 3 PCB Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R752, R753	Res, comp, 820 $\pm 5\%$, 1/4W	149484	01121	CB8215	2		
R754, R756, R757	Res, comp, 100K $\pm 5\%$, 1/4W	148189	01121	CB1045	3		
R758	Res, comp, 390 $\pm 5\%$, 1/4W	147975	01121	CB3915	1		
R764 thru R767	Res, comp, 4.7M $\pm 5\%$, 1/4W	220046	01121	CB4755	4		
U701, U705	IC, Array, NPN Si, 5-xstr	248906	86684	CA3046	2	1	
U702, U703, U706, U707	I.C. Lin Op Amp	363515	07263	LM301AN	4	1	
U704, U708, U709	I.C. CMOS, hex buffer/inv, 16 pin 	381830	95303	CD4050AE	3	1	
U710	Res, Ntwk, 13 - 100K $\pm 5\%$, 1/4W, 14 pin	404624	56289	Type 914C	1		
U711 thru U714	IC, TTL, Tri-state hex buffer	408146	07263	DM8095N	3		
 Indicates MOS device which maybe damaged by static discharge.							

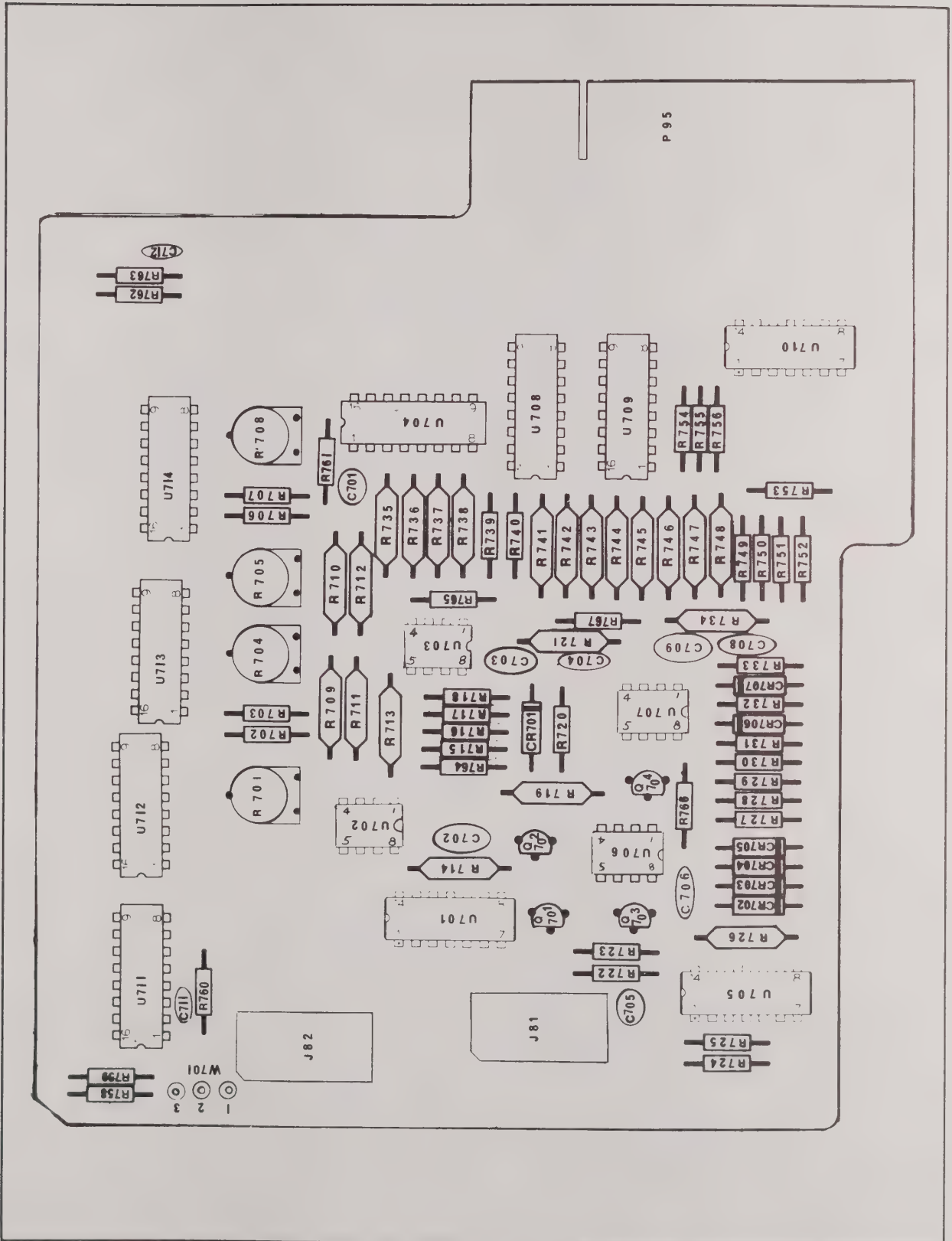


Figure 612-4. RCU 3 PCB Assembly

Option —13 1 GHz Prescaler

613-1. Introduction

613-2. The channel C input of the Model 1953A is intended for use with an optional frequency-prescaler. Option —13 is a prescaler which extends the operating range of the counter to 1 GHz. This prescaler has a frequency range extending from 50 MHz to 1 GHz with a specified sensitivity of 15 mV rms.

613-3. The option comprises a plug-in PCB assembly, a front-panel-mounted BNC connector, and the related components required both to adjust the power supply for correct operating voltages and to compensate the counter circuitry for the prescaling divisor. The Option must be ordered factory-installed in the 1953A when the instrument is purchased, it is not field installable.

613-4. Operation

613-5. Operation of the 1953A in the prescaler mode is established by rotating the FUNCTION switch to the FREQUENCY C position.

613-6. Theory of Operation

613-7. The main function of the prescaler is to reduce the frequency of the input signal to below 130 MHz for application to the main gate and decade counters. The prescaler also provides the necessary conditioning of the input signal to provide sufficient gain and the proper waveshaping. The frequency division factor for the 1 GHz prescaler is eight.

613-8. As shown in Figure 613-1, the input signal is fed through an input protection fuse, F1, to the input of the amplifier, which contains input limiting. The output of the amplifier, which is also internally limited, is applied to a divider circuit which divides by a factor of eight to reduce the input frequency to below 130 MHz. The prescaled signal, amplified by U1 and divided by U2 and U3 is fed to the main PCB assembly for application to the main gate and decade counters.

613-9. The output of the amplifier is sensed via CR1/U5, to detect signals whose level is too low to reliably clock the divider circuit. When a low signal level is detected, the divider output is disabled causing the display to read zero.

613-10. Performance Checks

613-11. The performance check for the 1 GHz prescaler is actually a sensitivity check made at the upper and lower frequency limits. Proceed as follows:

- a. Connect a 1 GHz RF generator, terminated into 50 ohms, to a T-connector on the CHANNEL C input. Set the generator output for 25 MHz at approximately 15 mV rms.
- b. Connect the RF millivoltmeter (Refer to Table 4-1) to the T-connector on the input of the prescaler.
- c. Adjust the generator output for a reading of 15 mV rms on the RF millivoltmeter.
- d. Confirm that the counter reads $25 \text{ MHz} \pm$ generator accuracy.
- e. Change the generator output to 1 GHz and adjust the output for 15 mV on the RF millivoltmeter.

613-12. Calibration

613-13. Calibration of the prescaler amounts to adjustment of the low level sense control located on the top edge of the prescaler PCB assembly. Proceed as follows:

- a. Remove the top dust cover from the instrument.
- b. Energize the counter and connect the RF generator to the CHANNEL C input connector. Select an output of 100 MHz at approximately 15 mV rms.
- c. On the counter, adjust the level control (R15) to a midpoint which produces a stable display.

- d. Reduce the input signal level until the display becomes unstable.
- e. Re-adjust the level control until the display is again stable.
- f. Repeat steps d and e until no additional sensitivity, can be achieved.

613-14. List of Replaceable Parts

613-15. Table 613-1 is a list of replaceable parts for the 1 GHz Prescaler. Refer to Section 5 for an explanation of the columnar entries. The component locations are illustrated in Figure 613-2.

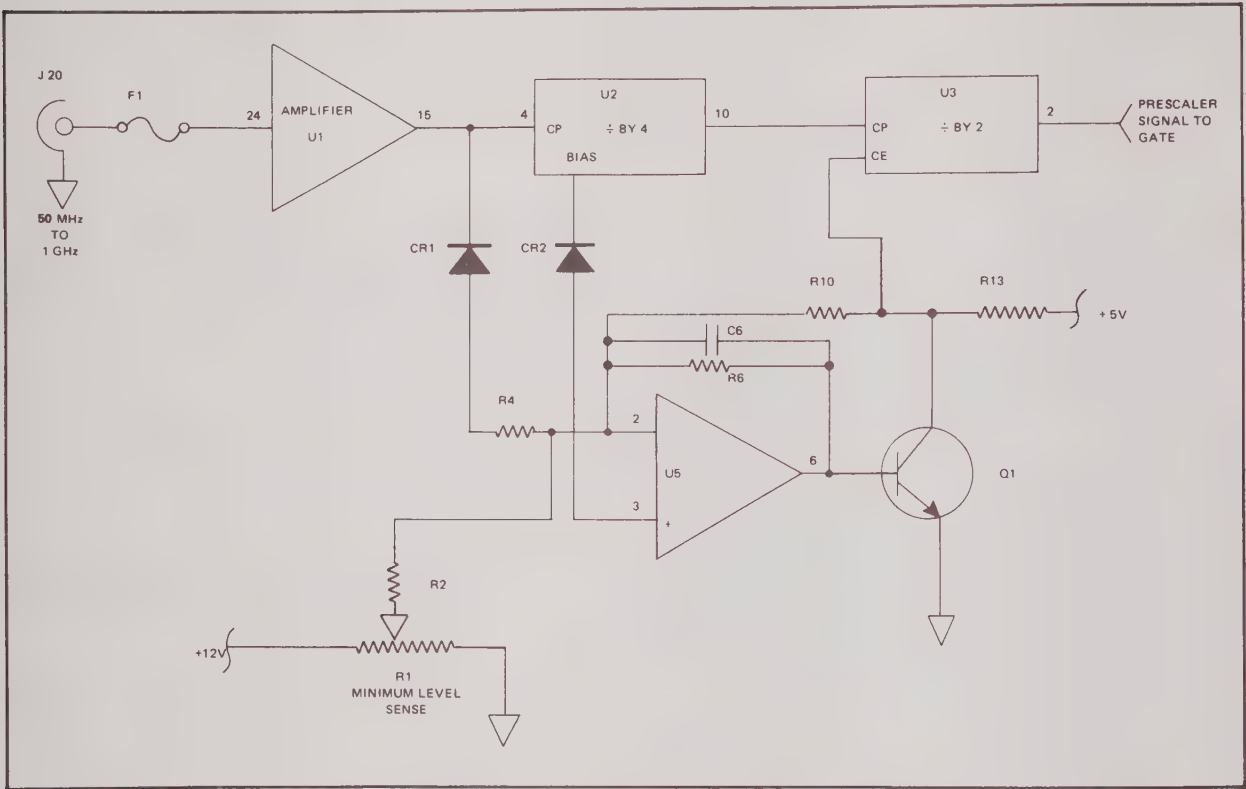


Figure 613-1. 1 GHz - Prescaler, Block Diagram

Table 613-1. 1000 MHz Prescaler Option –13

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U13	1000 MHz PRESCALER OPTION –13						
	1000 MHz Prescaler PCB Assembly	396309	89536	396309	1		
	Cable Assy (Front Panel to PCB)	406942	89536	406942	1		
	1000 MHz Decal	428037	89536	428037	1		
	IC, TTL, 4-bit Binary Counter (installed on the counter main PCB)	320739	01295	SN7493N	1	1	

Table 613-2. 1000 MHz Prescaler PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	1000 MHz PRESCALER PCB ASSEMBLY Option -13 Figure 613-2	396309	89536	396309	REF		
C1, thru C6, C8, C9	Cap, cer, 0.001 uF	402966	71590	8121-A100-W5	8		
C7, C10	Cap, cer, 0.001 uF $\pm 10\%$, 500V	357806	71590	CB102	2		
C11	Cap, tant, 10 uF $\pm 20\%$, 15V	193623	56289	196D106X000 15KA1	1		
CR1, CR2	Diode, Hot Carrier	369595	07263	GH1100	2	1	
F1, F2	Fuse, 0.2A, 2.6 ohms	370577	75915	273.200	2		
J20	Coax. Connector, Snap-on, PCB Mount Right Angle Con-Hex Type	353243	98291	51.053.000	1		
L1	Ferrite Bead	321182	02114	56-590-65-4B	1		
Q1, Q3	Xstr, NPN, Si, sm/sig	218396	04713	2N3904	2	1	
Q2	Xstr, PNP, sm/sig, Si	352369	07263	2N4403	1	1	
R1	Res, var 10K $\pm 20\%$	385393	54869	PT-10H-10K	1		
R2, R6	Res, comp, 330K $\pm 5\%$, 1/4W	192948	01121	CB3345	2		
R3, R5, R13, R17	Res, comp, 2.7K $\pm 5\%$, 1/4W	170720	01121	CB2725	4		
R4, R11	Res, comp, 10K $\pm 5\%$, 1/4W	148106	01121	CB1035	2		
R7, R8, R15	Res, comp, 470 $\pm 5\%$, 1/4W	147983	01121	CB4715	1		
R9	Res, comp, 4.7K $\pm 5\%$, 1/4W	148072	01121	CB4725	1		
R10, R18	Res, comp, 1K $\pm 5\%$, 1/4W	148023	01121	CB1025	2		
R14	Res, comp, 1.5K $\pm 5\%$, 1/4W	148031	01121	CB1525	1		
R16	Res, comp, 51 $\pm 5\%$, 1/8W	266262	01121	BB5101	1		
U1	IC, Hybrid Linear, Broad Band Ampl	428797	31091	CA1044	1	1	
U2	IC, ECL, Selected	444034	89536	444034	1	1	
U3	IC, TTL, D-type flip-flop	404574	07263	F11C06DC	1	1	

Table 613-2. 1000 MHz Prescaler PCB Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U4	IC, Op-Amp, MINI-DIP, 8 pin	402750	07263	LM741CN	1	1	
1	Connector, Test Jack	149112	74970	105-0753	2		
2	AMP Receptacle	375329	00779	85863-3	6		
3	Socket, Miniature	403642	00779	50863-B	28		
4	IC Socket, lp, 14 pin	291542	00779	583527-1	1		
5	IC Socket, lp, 16 pin	370312	01295	C931602	1		

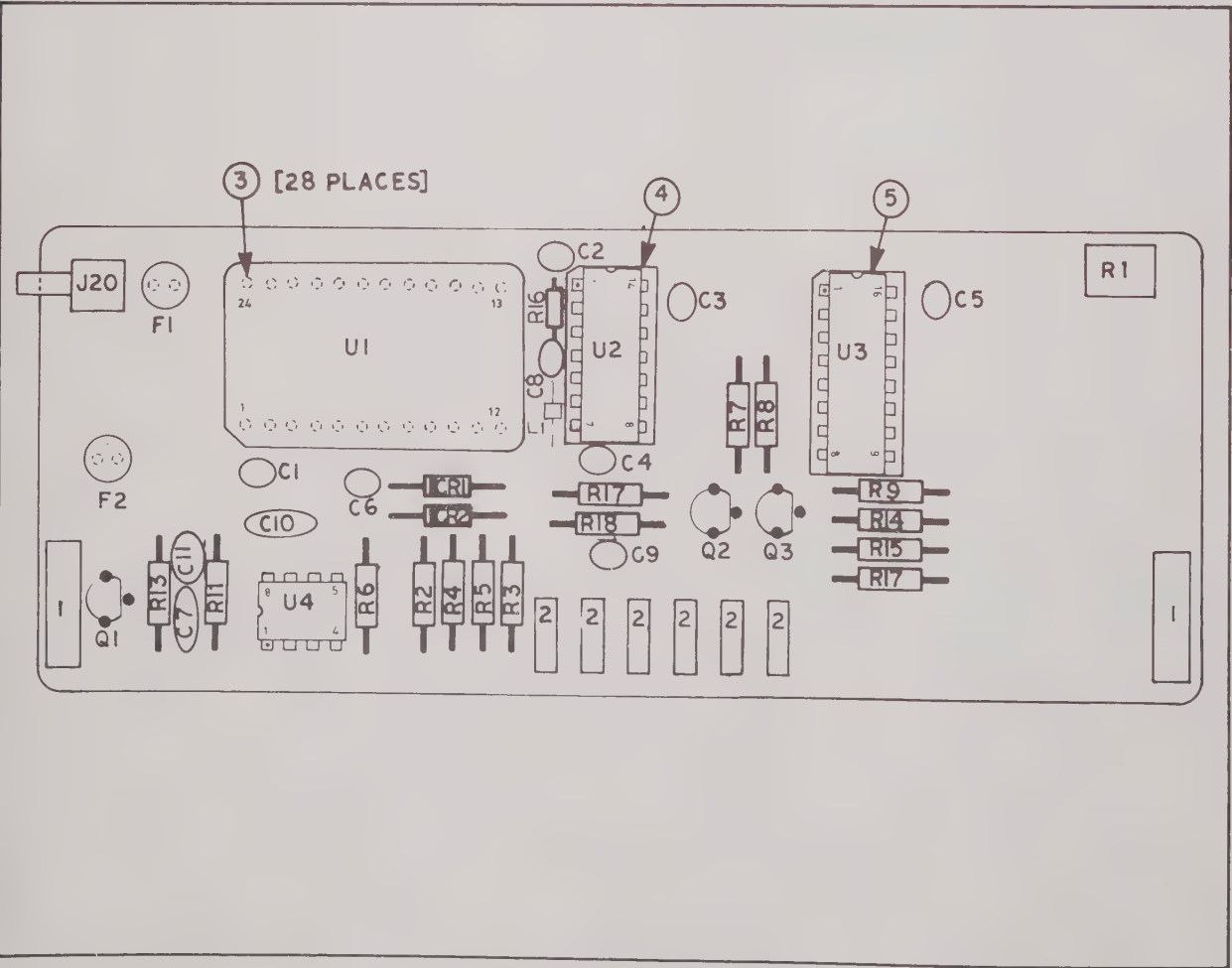


Figure 613-2. 1 GHz/1.25 GHz Prescaler

Option —14

1.25 GHz Prescaler

614-1. Introduction

614-2. The channel C input of the Model 1953A is intended for use with an optional frequency prescaler. Option —14 is a prescaler which extends the operating range of the counter to 1.25 GHz. This prescaler has a frequency range extending from 50 MHz to 1.25 GHz with a specified sensitivity of 15 mV rms from 50 MHz to 1 GHz decreasing to 30 mV rms between 1 GHz and 1.25 GHz.

614-3. The option comprises a plug-in PCB assembly, a front-panel-mounted BNC connector, and the related components required both to adjust the power supply for correct operating voltages and to compensate the counter circuitry for the prescaling divisor. The Option must be ordered factory-installed in the 1953A when the instrument is purchased, it is not field installable.

614-4. Operation

614-5. Operation of the 1953A in the prescaler mode is established by rotating the FUNCTION switch to the FREQ C position.

614-6. Theory of Operation

614-7. The main function of the prescaler is to reduce the frequency of the input signal to below 165 MHz for application to the main gate and decade counters. The prescaler also provides the necessary conditioning of the input signal to provide sufficient gain and the proper waveshaping. The frequency division factor for the 1.25 GHz prescaler is eight.

614-8. As shown in Figure 614-1, the input signal is fed through an input protection fuse, F1, to the input of the amplifier, which contains an input limiting. The output of the amplifier, which is also internally limited, is applied to a divider circuit which divides by a factor of eight to reduce the input frequency to below 165 MHz. The prescaled signal, amplified by U1 and divided by U2 and U3 is fed to

the main PCB assembly for application to the main gate and decade counters.

614-9. The output of the amplifier is sensed via CR1 and U5, to detect signals whose level is too low to reliably clock the divider circuit. When a low signal level is detected, the divider output is disabled causing the display to read zero.

614-10. Performance Checks

614-11. The performance check for the 1.25 GHz prescaler is actually a sensitivity check made at the upper and lower frequency limits. Proceed as follows:

- a. Connect a 1.3 GHz RF generator, terminated into 50 ohms, to a T-connector on the CHANNEL C input. Set the generator output for 50 MHz at approximately 15 mV rms.
- b. Connect the RF millivoltmeter (Refer to Table 4-1) to the T-connector on the input of the prescaler.
- c. Adjust the generator output for a reading of 15 mV rms on the RF millivoltmeter.
- d. Confirm that the counter reads 50 MHz $\pm$ generator accuracy.
- e. Change the generator output to 1.25 GHz and adjust the output for 30 mV rms on the RF millivoltmeter.
- f. Confirm that the counter reads 1.25 GHz $\pm$ generator accuracy.

614-12. Calibration

614-13. Calibration of the prescaler amounts to adjustment of the sense control located on the top edge of the prescaler PCB assembly. Proceed as follows:

- a. Remove the top dust cover from the instrument.
- b. Energize the counter and connect the RF generator to the CHANNEL C input connector. Select an output of 100 MHz at approximately 15 mV rms.

- c.

On the counter, adjust the level control (R15) to a midpoint which produces a stable display.
- d.

Reduce the input signal level until the display becomes unstable.
- e.

Re-adjust the level control until the display is again stable.
- f.

Repeat steps d and e until no additional sensitivity can be achieved.

614-14. List of Replaceable Parts

614-15. Table 614-1 is a list of replaceable parts for the 1.25 GHz prescaler. Refer to Section 5 for an explanation of the columnar entries. The component locations are illustrated in Figure 614-2.

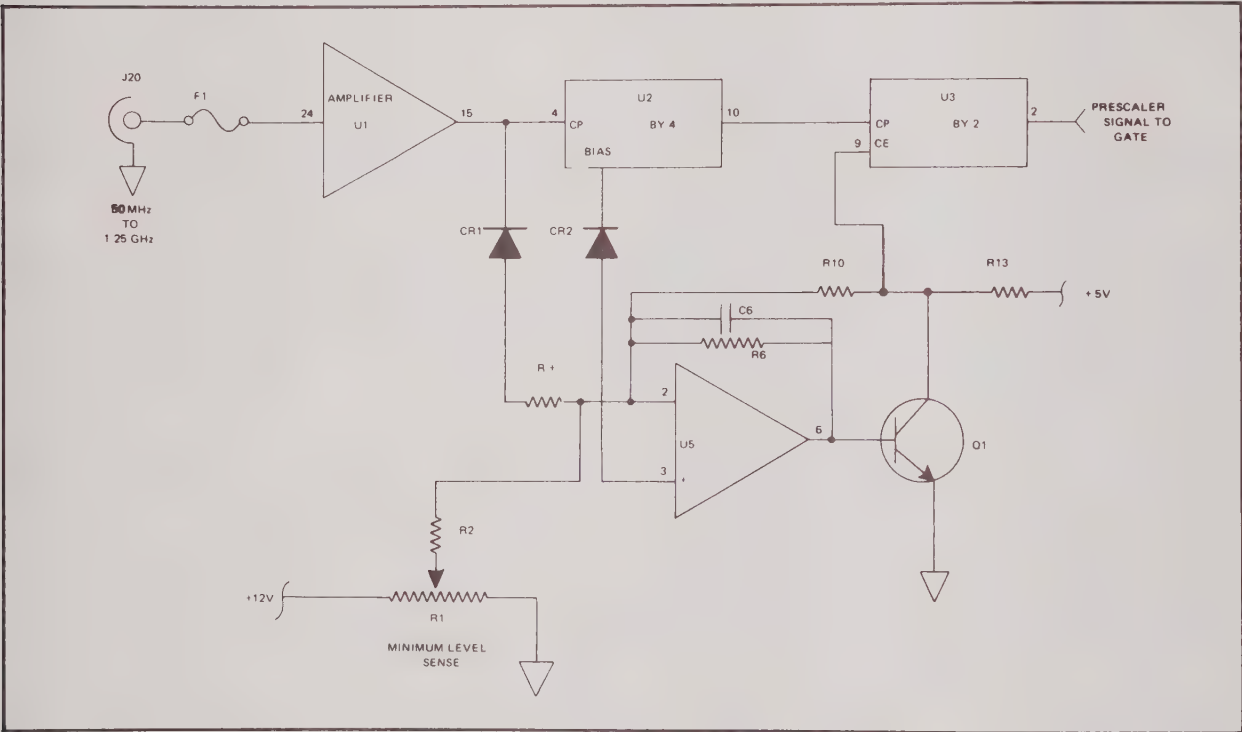


Figure 614-1. 1.25 GHz Prescaler, Block Diagram

Table 614-1. 1250 MHz Prescaler Option –14

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U13	1250 MHz PRESCALER OPTION –14						
	1250 MHz Prescaler PCB Assy	405597	89536	405597	1		
	Cable Assy (Front Panel to PCB)	406942	89536	406942	1		
	1250 MHz Decal	428045	89536	428045	1		
	IC, TTL, 4-bit binary counter (Installed on counter main PCB)	320739	01295	SN7493N	1	1	

Table 614-2. 1250 MHz Prescaler PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	1250 MHz PRESCALER PCB ASSEMBLY	405589	89536	405589	REF		
C1 thru C6, C8, C9	Cap, cer, 0.001 uF	402966	71590	8121-A100-W5 R-102M	8		
C7, C10	Cap, cer, 0.001 uF $\pm 10\%$, 500V	357806	71590	CB102	2		
C11	Cap, Tant, 10 uF $\pm 20\%$, 16V	193623	56289	196D106X000 15KA1	1		
CR1, CR2	Diode, hot carrier	369595	07263	DH1100	2	1	
F1, F2	Fuse, 0.2A, 2.6 ohms	370577	75915	273.200	2		
J20	Coax, connector, Snap-on, PCB Mount Right Angle Con-Hex Type	353243	98291	51-053-000	1		
L1	Ferrite Bead	321182	02114	56-590-65-4B	1		
Q1, Q3	Xstr, NPN, Si, sm/sig	218396	04713	2N3904	2	1	
Q2	Xstr, PNP, sm/sig, Si	352369	07263	2N4403	1	1	
R1	Res, var 10K $\pm 20\%$	385393	54869	PT-10H-10K	1		
R2, R6	Res, comp, 330K $\pm 5\%$, 1/4W	192948	01121	CB3345	2		
R3, R5, R13, R17	Res, comp, 2.7K $\pm 5\%$, 1/4W	170720	01121	CB2725	4		
R4, R11	Res, comp, 10K $\pm 5\%$, 1/4W	148106	01121	CB1035	2		
R7, R8, R15	Res, comp, 470 $\pm 5\%$, 1/4W	147983	01121	CB4715	3		
R9	Res, comp, 4.7K $\pm 5\%$, 1/4W	148072	01121	CB4725	1		
R10, R18	Rex, comp, 1K $\pm 5\%$, 1/4W	148023	01121	CB1025	2		
R14	Res, comp, 1.5K $\pm 5\%$, 1/4W	148031	01121	CB1525	1		
R16	Res, comp, 51 $\pm 5\%$, 1/8W	266262	01121	BB5101	1		
U1	IC, Hybrid, Linear Broad Band Ampl	428797	31091	CA 1044	1		
U2	IC, ECL, selected	418186	89536	418196	1	1	
U3	IC, TTL, D-type, flip-flop	404574	07263	F11C06DC	1	1	
U4	IC, Op-Amp, MINI-DIP, 8 pin	402750	07263	LM741CN	1	1	

Table 614-2. 1250 MHz Prescaler PCB Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
1	Connector, Test Jack	149112	74970	105-0753	2		
2	AMP Receptacle	375329	00779	85863-3	6		
3	Socket, Miniature	403642	00779	50863-B	28		
4	IC Socket, L.P., 14 pin	291542	00779	582527-1	1		
5	IC Socket, L.P., 16 pin	370312	01295	C931602	1		

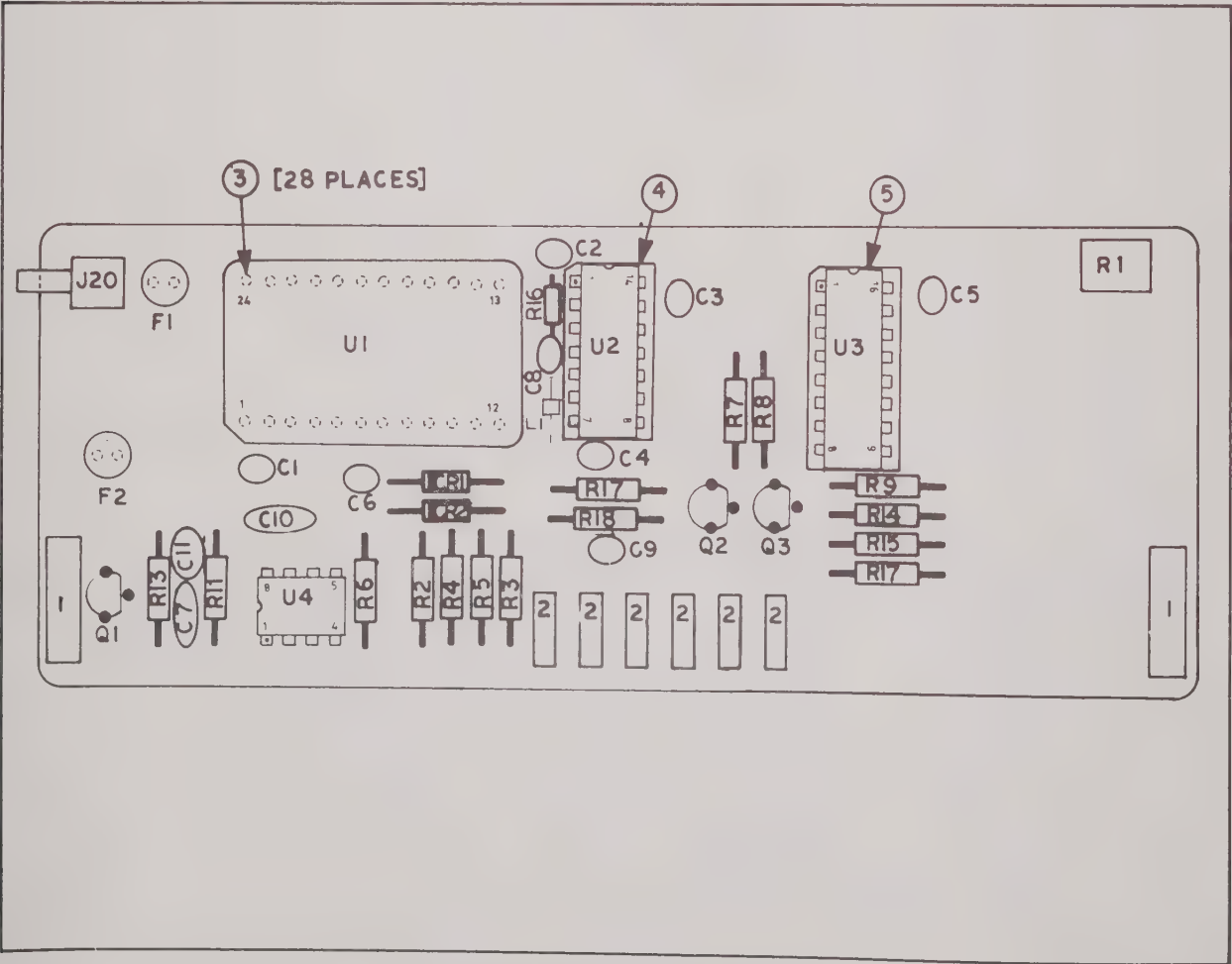


Figure 614-2. 1 GHz/1.25 GHz Prescaler

Option —15 IEEE-488 Standard Interface

615-1. Introduction

615-2. Option —15 is an IEEE-488 standard interface which uses the subsets SH1, AH1, T5, TE0, L4, LE0, SR1, RL2, PP0, DC0 and DT0. All programming of the counter is based on a character-serial, seven bit ASCII code, using 26 of the character set. All other characters are ignored by the interface. Status may be requested and an alphanumeric coded response of the status obtained.

615-3. By entering commands from a control device a measurement response can be obtained, either continuously or on command. The measurement response includes nine digits of data, with an embedded decimal point and an exponent. An overflow indication is included when the response exceeds the numeric display of the instrument. The status of the counter can be obtained by requesting a Status Response Message from the interface. The reply is a single character, in an alphanumeric code.

615-4. Specifications

615-5. The specifications for the IEEE interface are: full remote programming of function, range, and all signal conditioning controls including trigger levels. Directly compatible with IEEE Interface Standard. Data output includes 9 digits of display information, decimal point and exponent for time or frequency units. Front panel lockout is provided. An application bulletin covering the programming of this option is available upon request.

615-6. Installation

615-7. If the IEEE-488 Standard Interface, Option —15 is desired, it must be installed at the factory. The option is not field-installable.

615-8. Operating Features

615-9. Installation of Option —15 in the instrument adds the Operator switches shown in Figure 615-1. A1 through A5 are used to control the local address of the counter.

They may be set to the binary equivalent of any number, 0 through 30. The number 31 (11111) is reserved for the “unlisten” instruction which tells the counter to output continuously. The A1 through A5 switches are placed toward the top for a binary 1. Set the address of the counter using the codes in Table 615-1.

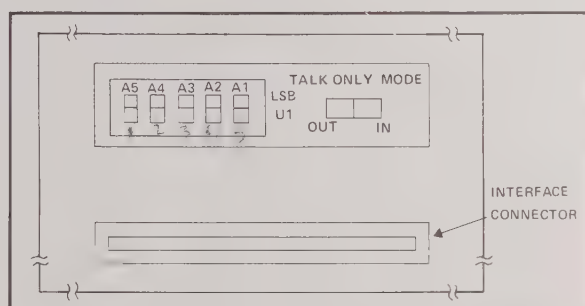


Figure 615-1. IEEE Address Switches

615-10; The TALK ONLY MODE switch controls whether the counter will operate as a “talker” only or as both a “Talker” and “Listener.” With the switch to the right (IN), the counter only “Talks.”

615-11. Differentiation on the bus between “Talk”, “Listen” and commands is made by the controller as it manipulates the two high order bits of the seven controlling lines.

615-12. OPERATING NOTES

615-13. Commands

615-14. The commands can be subdivided into Operating Functions, Range, Trigger Instructions, Coupling, Output Functions, Sampling, Status and Clear. An explanation and breakdown of these commands and their respective codes are given in the following sub-paragraphs.

615-15. Operating Function Commands

615-16. This group of commands provide for the selection of the operating function. The commands correspond to the

positions of the FUNCTION switch on the front panel. The commands and their applicable codes are listed in Table 615-2.

Table 615-1. Allowable Listen and Talk Addresses

DECIMAL	5 4 3 2 1 B I N A R Y	ASCII CHARACTER	
		LISTEN	TALK
0	0 0 0 0 0	SP	@
1	0 0 0 0 1	!	A
2	0 0 0 1 0	"	B
3	0 0 0 1 1	#	C
4	0 0 1 0 0	\$	D
5	0 0 1 0 1	%	E
6	0 0 1 1 0	&	F
7	0 0 1 1 1	'	G
8	0 1 0 0 0	(	H
9	0 1 0 0 1	)	I
10	0 1 0 1 0	*	J
11	0 1 0 1 1	+	K
12	0 1 1 0 0	,	L
13	0 1 1 0 1	-	M
14	0 1 1 1 0	.	N
15	0 1 1 1 1	/	O
16	1 0 0 0 0	0	P
17	1 0 0 0 1	1	Q
18	1 0 0 1 0	2	R
19	1 0 0 1 1	3	S
20	1 0 1 0 0	4	T
21	1 0 1 0 1	5	U
22	1 0 1 1 0	6	V
23	1 0 1 1 1	7	W
24	1 1 0 0 0	8	X
25	1 1 0 0 1	9	Y
26	1 1 0 1 0	:	Z
27	1 1 0 1 1	;	
28	1 1 1 0 0	<	\
29	1 1 1 0 1	=	]
30	1 1 1 1 0	>	^

Table 615-2 Operating Functions

CODE	FUNCTION
F0	Freq A
F1	Freq C
F2	Freq (A/B)
F3	Period A
F4	T.I. A-B
F5	A GTD By B
F6	Self-Check

615-17. Range Commands

615-18. The Range Commands are listed in Table 615-3. Each code corresponds to a switch position on the front panel RANGE switch.

615-19. Trigger Instructions

615-20. The trigger for channel A and channel B can be programmed for both level and function. The function includes positive or negative slope and AC or DC coupling. The trigger levels are variable with either a positive or negative reference between 0.01 and 0.99 volts with 0.01 volt resolution and between 0.1 and 9.9 volts with 0.1 resolution. The commands correspond to the switches in the applicable channel Trigger controls and Signal conditioners. Table 615-4 contains the Trigger Codes and their instructions.

Table 615-3. Range Commands

CODE	RANGE		
	GATE T.	PER AVGD	T.I. RES
R0	0.1 ms	10 ⁰	0.1 us
R1	1.0 ms	10 ¹	1.0 us
R2	10 ms	10 ²	10 us
R3	0.1 s	10 ³	0.1 ms
R4	1.0 s	10 ⁴	1.0 ms
R5	10 ss	10 ⁵	10 ms

Table 615-4. Trigger Instructions

CODE		
CHANNEL A	CHANNEL B	INSTRUCTION
A+	B+	Positive Slope
A-	B-	Negative Slope
A0	B0	AC Coupled
A1	B1	DC Coupled
A+0	B+0	Positive Slope and AC Coupled
A+1	B+1	Positive Slope and DC Coupled
A-0	B-0	Negative Slope and AC Coupled
A-1	B-1	Negative Slope and DC Coupled
LA+X.X	LB+X.X	Trigger level of +X.X Volts
LA-X.X	LB-X.X	Trigger level of -X.X Volts
LA+.XX	LB+.XX	Trigger level of +.XX Volts
LA-.XX	LB-.XX	Trigger level of -.XX Volts
X = numeric digit 0 through 9. If only the first digit is substituted for the "X" the second must be replaced with a termination character.		

615-21. Coupling

615-22. To couple channel A and channel B, program the instruction S1. Programming the instruction S0 separates channel A and B. The front panel equivalent is the SEP-COM switch between the two channel areas.

615-23. SAMPLING INSTRUCTIONS

615-24. The sample rate can be programmed with either the H0 or H1 code. The data is sampled continuously with H0 programmed; while with H1 it is sampled only on request. The code required to trigger a sample with H1 programmed is the character T.

615-25. Output Functions

615-26. The Output Modes are programmed using a code of M0 or M1. When programmed with a M0 code, the 1953A outputs the last frequency measured when it is addressed and then resumes taking measurements at the rate set by the Sampling Instructions, either H0 or H1. For the M1 code, the 1953A outputs a service request (SRQ) on the bus after it has taken a measurement, then waits until it is addressed to transmit that measurement. After transmission of the measurement, the 1953A resumes sampling at the rate programmed by the Sampling Instruction.

615-27. When both the H1 and M1 codes are programmed, the code X causes the retransmission of the last reading.

615-28. Status Instruction

615-29. With the code character G programmed and the Interface addressed as a "Talker," the 1953 outputs a status response. The format of the responses is detailed in a later paragraph.

615-30. Clear Command

615-31. Programming the code character C initializes the instrument to the following:

F0 R0 A+0 B+0 LA.00 LB.00 S0 M0 H0,

This is the equivalent of: Frequency A at the 0.1 ms range; channel A positive slope, ac coupled; channel B positive slope, ac coupled; channel A trigger level of +.00 Volts; channel B trigger level of +.00 Volts; channel A and B separated; output when addressed; and sample continuously.

615-32. Programming Example

615-33. A typical command and an explanation of each section is given in Table 615-5.

Table 615-5. Programming Example

Example: F4 R1 LA-2.7 LB.85 A-1 B1 S0	
CODE	INSTRUCTION
F4	Time Interval
R1	1 usec Resolution
LA-2.7	A trigger level at -2.7 Volts
LB.85	B trigger level at +.85 Volts
A-1	Channel A, Negative Slope, Direct Coupling
B1	Channel B, Positive Slope, Direct Coupling
S0	Channels A and B Separate

615-34. INTERFACE RESPONSES

615-35. Measurement Response

615-36. The format of the measurement response is shown in Figure 615-2. The response is transmitted when the interface is addressed while in the proper mode.

615-37. Status Response

615-38. A request for status brings a response of a one-digit status message, followed by the carriage return and line feed termination characters. Refer to the applicable columns of Table 615-6 for the status of the Gate, Overflow and Busy Signals.

615-39. Status Response in Serial Poll Mode

615-40. A request for a status response in the Serial Poll mode results in a single character reply without any termination characters. Refer to the applicable columns of Table 616-6 for the status of the Gate, Overflow, Busy and Service Request Signals.

615-41. The Serial Poll status request instruction is dependent upon the controlling device and the IEEE bus. Refer to the standard and the sub-set used for this information.

615-42. THEORY OF OPERATION

615-43. The theory of operations for the IEEE 488 Interface is given in the following paragraphs on a block diagram level. The description includes an explanation of the operation of the interface in both the listen and talk modes since the counter is capable of both listening (accepting commands to change range, status, function, etc.) and talking (transmitting measurement or status information) to the bus. The counter is assigned through the interface a five bit address, which is the five low order bits of an ASCII character. The two high order bits determine whether it is to be a talk

or listen address. Refer to Table 615-6 for the addresses available. The address 1111 is reserved for the “unlisten” and “untalk” commands which prevent the counter from misunderstanding the information on the bus and talking or listening to itself. The block diagram of the interface used in the discussion is found in Figure 615-3.

615-45. To operate in the Listen Mode, the pre-selected address must be on the Data Lines and the REN and ATN command lines active. This action, followed by active DAV and RFD signals, sets control flip flops in the Data Decoders and Control Storage, preparing the interface microprocessor to accept instructions from the controller. After the data has been accepted, the DAC lines become active, inactivating ATN and DAV. The last action results in the DAC signal

These Columns Are Applicable To Status Response.					
STATUS	GATE OPEN	OVERFLOW	COUNTER BUSY	SERVICE REQUEST	SERIAL POLL STATUS
0	NO	NO	NO	NO	!
0	NO	NO	NO	YES	a
1	NO	NO	YES	NO	#
1	NO	NO	YES	YES	c
2	NO	YES	NO	NO	%
2	NO	YES	NO	YES	e
3	NO	YES	YES	NO	,
3	NO	YES	YES	YES	g
4	YES	NO	NO	NO	)
4	YES	NO	NO	YES	i
5	YES	NO	YES	NO	+
5	YES	NO	YES	YES	k
6	YES	YES	NO	NO	-
6	YES	YES	NO	YES	m
7	YES	YES	YES	NO	/
7	YES	YES	YES	YES	0
				These Columns Are Applicable To Status Response in Serial Poll Mode.	

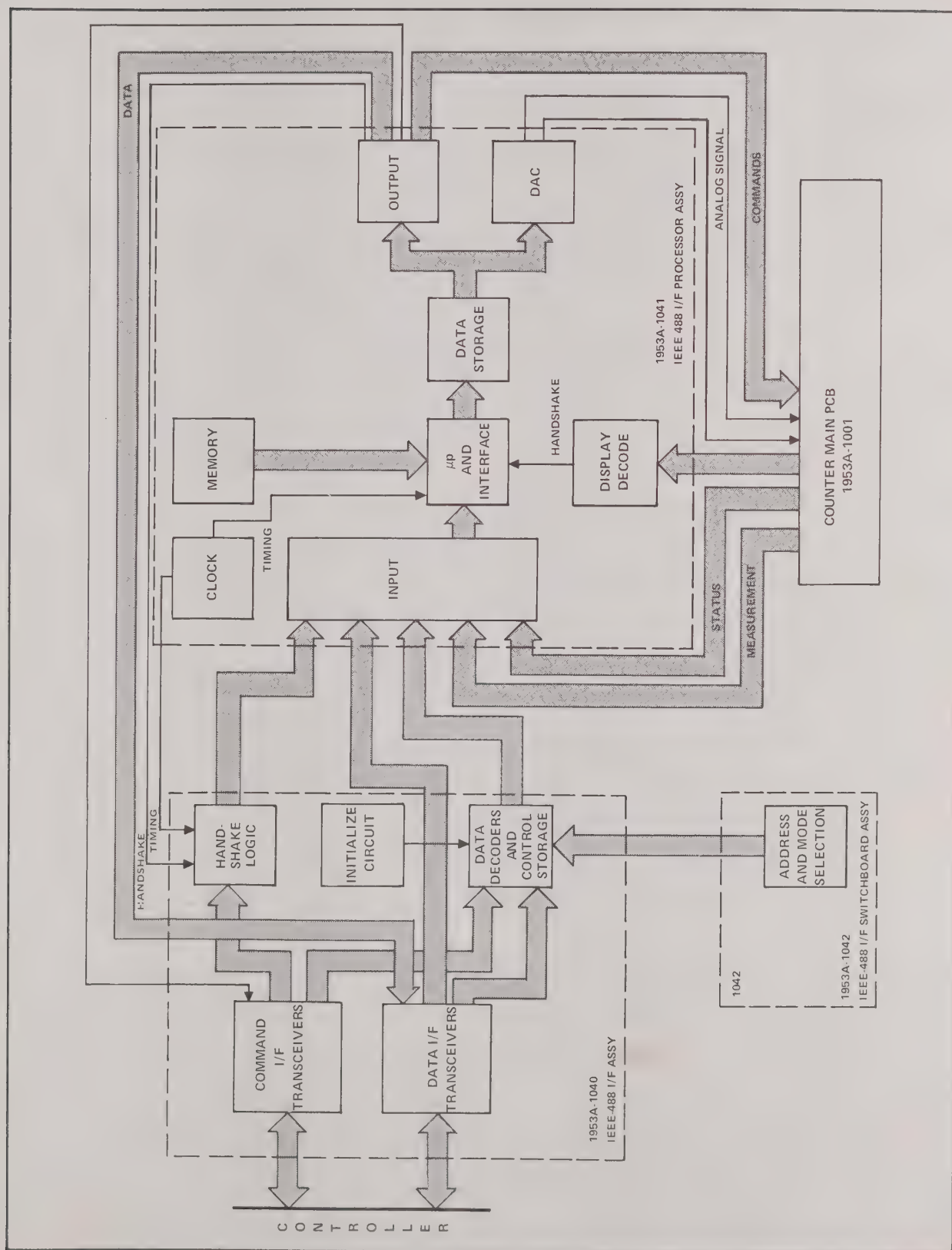


Figure 615-3. IEEE Interface Block Diagram

returning to inactive so that the interface is now ready to accept instructions.

615-46. Starting an instruction requires the ASCII code for the desired instruction on the data lines with ATN inactive and RFD active. The Controller drives DAV active to start the Handshake sequence. Once the data has been accepted in the microprocessor, the DAC signal goes active to complete the Handshake sequence. The microprocessor acts on the instruction, transforms it into the digital format required and outputs the instruction to the counter, passing through the digital-to-analog converter or stored pending a complete instruction, if required.

615-47. Talk Mode

615-48. The Talk Mode requires the ATN signal active and the correct address, just as the Listen Mode, to differentiate between it and an instruction. The start of the Handshake sequence latches the command into the Data Decoders and Control Storage for transfer to the microprocessor. Once the Handshake sequence is complete, the interface is in the Talk mode and can begin transmitting data to the Controller.

615-49. After the addressing has been completed, the microprocessor accepts the data on the lines from the counter and outputs it through Data Storage to the Data I/F Transceivers and Controller. After completion, dependent upon the mode selected, it will either continue to transmit the outputs from the counter or, after the single sample be reset by the controller to hold until addressed again.

615-50. Talk-Only Mode

615-51. The I/F Switchboard assembly has a switch that allows the operator to place the instrument in the Talk-Only

Mode. In this configuration, the interface outputs the data from the counter, either measurement or status, as determined by a previous mode instruction or by the default configurations.

615-52. TROUBLESHOOTING

615-53. The use of microprocessor control in the IEEE-488 option increases the speed and efficiency of the interface but at the same time increases the complexity and difficulty of troubleshooting. The two significant pcb's in the interface are layered parallel to the counter main pcb. As a result, if any checks are required on the Interface pcb, the I/F processor pcb must be removed from the counter and reconnected back into the circuit using the extender cables available in the optional extender cable accessory kit 1953A-7020K. For this reason checkpoint locations are given on the I/F Processor pcb whenever feasible to preclude removal of the pcb until required.

615-54. Troubleshooting for the 1953A Option 15 IEEE Interface consists of the Tabular Flow Chart in Table 615-7. When a step on the flow chart is completed, check for a decision transfer. If no decision is required, perform the next step of the table in sequence.

615-55. LIST OF REPLACEABLE PARTS

615-56. Table 615-9 is a list of replaceable parts for the IEEE 488 Interface Option. Refer to Section 5 for an explanation of the columnar entries.

Table 615-7. IEEE-488 Troubleshooting (Continued)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
	<i>Note:</i> <i>The Microprocessor group called out in this procedure consists of the Clock U28, the 4040 Microprocessor U22, the ROM U23, the Memory Interface U17 and the Multiplexers U8, U13, U18 and U24. Due to the speed and complexities of these components, the recommended solution for troubleshooting is substitution.</i>		
1.	Address the counter with the assigned Listen address.		
2.	Check MLA at U18-1 with a Scope (Logic Tester).		
3.	Is the signal HIGH?	5	4
4.	Check the circuits on the Interface pcb. Verify that ATN is low at the input, then check the transceivers, addressing circuits, the handshake circuits and the listen flip-flop. Repair as required; then restart at Step 1.		
5.	If the controller in use will allow it, alter the listen address to the complement of the normal address to ensure the data transceivers will respond to both signal levels, e.g., if the normal listen address as shown in Table 615-1 is "/" for a binary code of 01111, change the address to "0" for a binary code of 10000, forcing the transceivers to go both high and low. Repeat Steps 1 through 4 with the new address, then return to the normal address and proceed to Step 6. If the address is not alterable, proceed to Step 6.		
6.	Perform the test in Table 615-8, checking for the applicable logic level with a scope.		
7.	Were all readings satisfactory:	9	8
8.	If the output of either U25 or U26 is incorrect, decode and check the signal input from U9, U10, U14 and U15. The data for U32 should be latched into U9, U10, U14 and U15 also. Check the applicable latch and controls if only the signals from that latch are affected. If these areas are satisfactory, check the microprocessor group. Repair as required, then repeat the applicable portions in Step 6.		
9.	Enter the instruction LA9.9 LB 9.9.		
10.	With a DVM or scope check at U12-4 (channel A) and U11-4 (channel B) for a voltage approaching 1 Vdc.		
11.	Enter the instruction LA.00 LB.00.		
12.	Check at U12-4 and U11-4 for a voltage approaching 0 Vdc.		
13.	Are the readings in Steps 10 and 12 correct?	15	14
14.	If the problem is in channel A, check the binary coded input to U3 from U14-9, U15-9, U9-9, U10-9 (first four bits) and U14-10, U15-10, U9-10, U10-10 (last four bits). For channel B, check the binary coded input to U5 from pins 11 and 12 of U14, U15, U9 and U10 for the first and last four bits, respectively. U14-9 and U14-11 are high for positive entries and low for negative. The remaining seven bits will start with all low for positive entries and increment for each count. Negative numbers will start with all high except the MSB at zero and decrement		

Table 615-7. IEEE-488 Troubleshooting (Continued)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
	one bit for each negative count. If these areas are satisfactory, check the microprocessor group. Repair as required, then repeat the test starting at Step 9.		
15.	Enter the instruction H0 M0.		
16.	Observe U20-13 with a scope for a pulse train.		
17.	Leave the scope connected to U20-13 and observe the display while entering the instruction H1.		
18.	The pulse train should cease with the completion of the entry.		
19.	Enter the instruction T.		
20.	One pulse should occur concurrent with the entry.		
21.	Enter the instruction H0.		
22.	The pulse train should resume with the completion of the instruction.		
23.	Are the indications in Steps 16 through 22 correct?	25	24
24.	Verify the operation of U20 and the microprocessor group. Repair as required, then restart the test at Step 16.		
25.	Enter the talk address.		
26.	Does the counter respond with measurement data to the controller?	31	27
27.	Monitor U21-10/U29-13 with a scope while entering the talk address.		
28.	Does the point pulse to a low logic level?	30	29
29.	Check at U18-1 for a High MTA. If MTA is not correct, check the circuits on the Interface pcb; ATN, the transceivers, addressing gates, handshake circuitry and the talk flip-flop. Repair as required, then repeat starting at Step 25.		
30.	Check the microprocessor group and U21/U29 with their associated circuitry. Repair as required then repeat starting at Step 25.		
31.	Enter the Listen address and the instruction H1 M1.		
32.	Address the instrument as a talker.		
33.	Record the transmitted measurement, if not done automatically by the controller.		
34.	Enter the Listen address and the instruction X.		
35.	Address the instrument as a talker.		
36.	Is the response the same as obtained in Step 33?	38	37
37.	Check the microprocessor group. The remaining circuits have been verified by previous tests. Repair as required, then restart at Step 31.		
38.	Enter the Listen address and the instruction G.		
39.	Address the instrument as a talker.		
40.	Is the one-digit status response correct?	42	41

Table 615-7. IEEE-488 Troubleshooting (Concluded)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
41.	Check the microprocessor group and the gate and overflow inputs from the main pcb. The remaining circuits have been verified by previous tests. Repair as required, then restart at Step 38.		
42.	Troubleshooting of the IEEE-488 interface is complete.		

Table 615-8. Instruction Logic Levels

Instruction Mnemonic		Logic Level High at	Logic Level Low at	Comments
Clear (C)	F0	U26 Group	U26-2	A high logic level for the U26 group infers that from the designated pins U26-2 through U26-7 and U26-9, all are high except the one specifically designated low. The same hold true for the U25 group which are pins U25-2 through U25-7.
	R0	U25 Group	U25-2	
	$\overline{SC}$		U32-11	
	$\overline{SA}$		U32-13	
	$\overline{DA}$		U32-3	
	$\overline{SB}$		U32-15	
	$\overline{DB}$		U32-7	
	$\overline{TA}$		U35-5	
	$\overline{TB}$		U32-9	
Freq C (F1)	$\overline{C}$	U26 Group	U26-3	
Freq A/B (F2)	$\overline{A/B}$	"	U26-4	
Period A(F3)	$\overline{PA}$	"	U26-5	
Time Interval (F4)	$\overline{TI}$	"	U26-6	
Agated by B(F5)	$\overline{AXB}$	"	U26-7	
Self Check (F6)	$\overline{CH}$	"	U26-9	
Freq A (F0)	$\overline{A}$	"	U26-2	
1.0 ms (R1)	$\overline{2}$	U25 Group	U25-3	
10.0 ms (R2)	$\overline{3}$	"	U25-4	
0.1 s (R3)	$\overline{4}$	"	U25-5	
1.0 s (R4)	$\overline{5}$	"	U25-6	
10.0 s (R5)	$\overline{6}$	"	U25-7	
0.1 ms (R0)	$\overline{1}$	"	U25-2	
Com (S1)	$\overline{SC}$	U32-11		
Sep (S0)	$\overline{SC}$		U32-11	
Slope A (A-1)	$\overline{SA}$		U32-13	
Neg DC Coupled	$\overline{DA}$		U32-3	
Slope A Pos AC Coupled (A+0)	$\overline{SA}$	U32-13		
	$\overline{DA}$	U32-3		
Slope B Neg DC Coupled (B-1)	$\overline{SB}$		U32-15	
	$\overline{DB}$		U32-7	
Slope B Pos AC Coupled (A+0)	$\overline{SB}$	U32-15		
	$\overline{DB}$	U32-7		
Ch AX10 (LA 0.0)	$\overline{TA}$		U32-5	
Ch AX1 (LA.00)	$\overline{TA}$	U32-5		
Ch BX10 (LB0.0)	$\overline{TB}$		U32-9	
Chan BX1 (LB.00)	$\overline{TB}$	U32-9		

Table 615-9. IEEE-488 Interface Option —15

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	IEEE-488 Interface Option-15 Note: Contains additional items for the Model 1953A Final Assembly RCU1 PCB Assy. (Table 615-10)  RCU2 PCB Assy. (Table 615-11)  Bus Interface PCB Assy. (Table 615-12) Processor PCB Assy. (Table 615-13) Switchboard PCB Assy. (Table 615-14) Support, Connector Screw, Connector Mounting	396242 396259 440214 440222 440230 439190 429472	89536 89536 89536 89536 89536 89536 89536	396242 396259 440214 440222 440230 439190 429472	1 1 1 1 1 1 2		
	Replace Input PCB Assy. A4 P/N 396127						

Table 615-10. RCU 1 PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	RCU 1 PCB ASSEMBLY						
	Option —15 Figure 615-4	396242	89536	396242	REF		
DS401 thru DS404	LED	385898	28480	5082-4487	4	1	
J1	Connector, Blck, PCB Test	149112	74970	105-0753	2		
	Receptacle	375329	00779	85863-3	12		
P10	Connector Post Uninsulated	376574	00779	5166-333-68	7		
R410 thru R413	Res., comp, $47 \pm 5\%$, $\frac{1}{4}W$	147892	01121	CB4705	4		
S108 thru S114	Slide Sw., SPDT	380113	79727	GF-124-SPDT	7	2	
U401	Res., Ntwk.-7 $10K \pm 5\%$, 1.5W	364000	71450	760-1	1	1	
U402	I.C., TTL, Hex Inc. Open Coll	379305	01295	SN7405N	1	1	

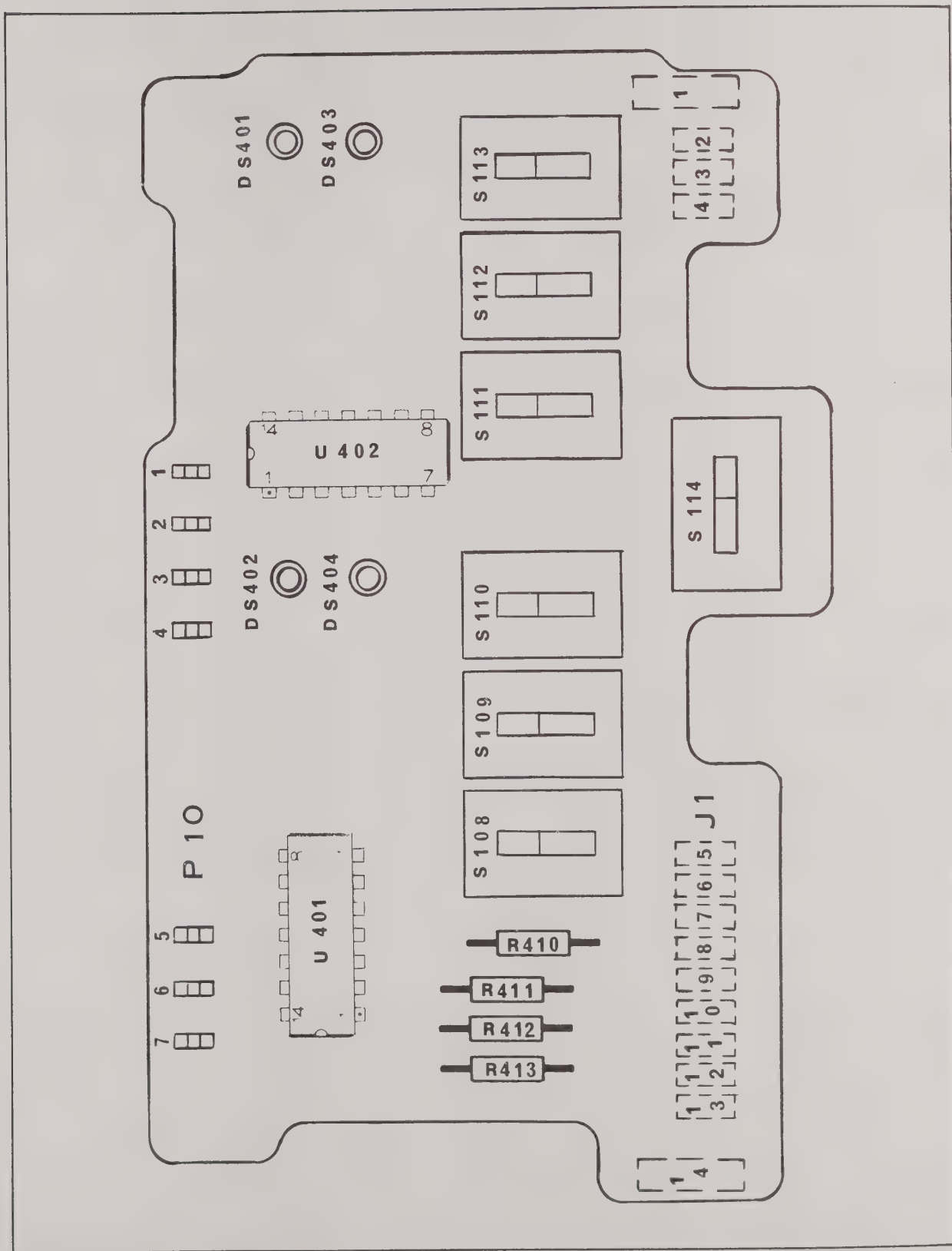


Figure 615-4. RCU 1 PCB Assembly

Table 615-11. RCU 2 PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	RCU 2 PCB ASSEMBLY						
	Option –15 Figure 615-5	396259	89536	396259	REF		
A404 thru A411	Rely, Dry Reed Monostable, SPST, 65mW, 380 ohms, 10%	334920	24211	GB-831A-4E	8		
C401, C402	Cap., Mylar 0.1 uF $\pm$ 10%, 250V	161992	73445	C280AE/N00K	2		
C403, C404	Cap, cer, 1.5 pF $\pm$ 0.25 pF, 1 kV	178475	56289	10TCCV15-NPO	2		
J2	Conn Test Jack, Blk.	149112	74970	105-0753	2		
	Receptacle	375329	00779	85863-3	9		
R401, R402	Res., comp, 910K $\pm$ 5%, ¼W	285338	01121	CB9145	2		
R403, R404	Res., comp, 100K $\pm$ 5%, ¼W	148189	01121	CB1045	2		
R405, R406	Res., Var., 10K ½W $\pm$ 30%	385880	89536	385880	2		
U403	I.C. TTL, Hex Inv., Open Coll	379305	01295	SN7405N	1	1	

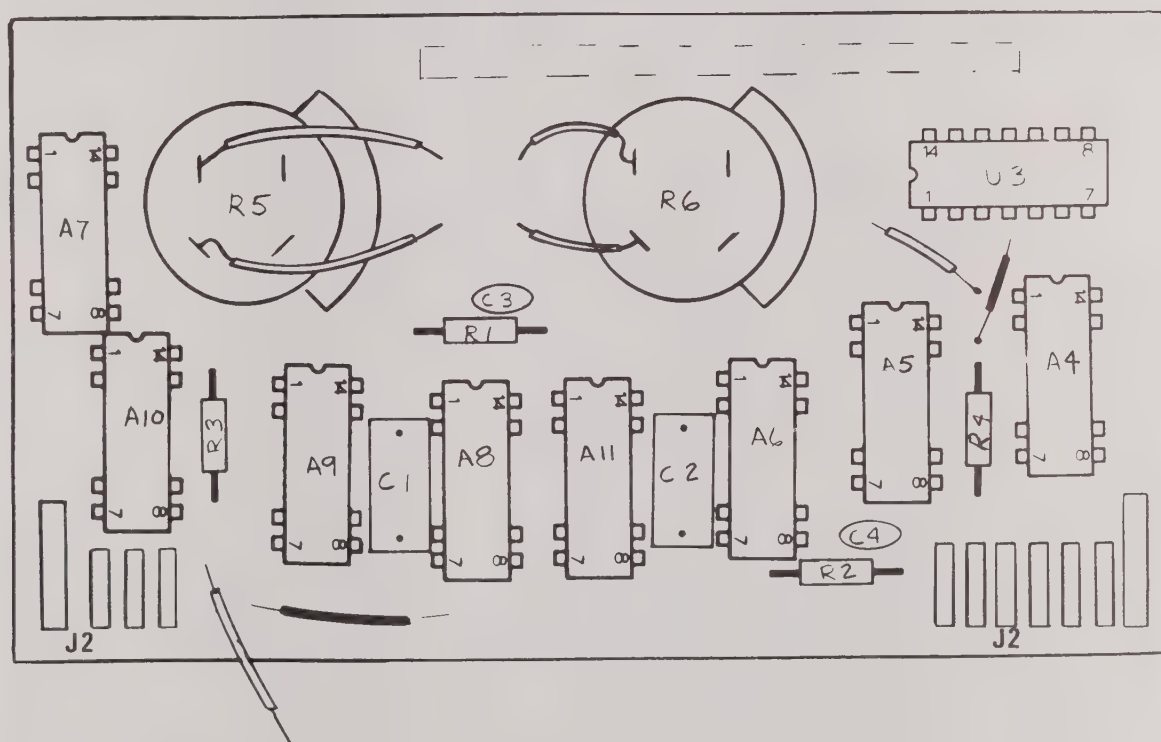


Figure 615-5. RCU 2 PCB Assembly

Table 615-12. Bus Interface PCB Assembly

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	IEEE-488 I/F Option—15 Bus Interface PCB Figure 615-6						
C1 thru C4	Cap, Ta, 0.22F, $\pm 20\%$, 35V	161331	56289	I96D224X 0035HAI	4		
C5	Cap, Mylar, 0.1 uF	393439	73445	C280MAH/A100K	1		
J1	Connector, female	408898	13511	57-20240-2 (323)	1		
J2, J3	Cable Assy.	380576	89536	380576	2		
J6	Socket, I.C., 16 pin	370312	01295	C931602	1		
R1	Res, fxd, comp, 390, $\pm 5\%$, $\frac{1}{4}W$	147975	01121	CB3905	1		
R2	Res, comp, 3K $\pm 5\%$, $\frac{1}{4}W$	193508	01121	CB3025	1		
U1 thru U4	I.C., Dig, Quad Interface Bus Transceiver	428649	04713	MC3446P	4	1	
U5, U6	I.C., TTL, Dig, Hex Inverter	393058	01295	SN74LS04N	2	1	
U7, U8, U13	I.C., TTL, Dig, Dual, J-K Neg-edge Triggered Flip-Flop	393157	01295	SN74LS107N	3	1	
U9, U10, U15, U19	I.C., TTL, Dig, Pos-NOR Gates 8 insul.	404889	01295	SN74LS30N	4	1	
U11, U14, U17	I.C., TTL, Dig, Pos-NOR Gates, Totem Pole Outputs	393041	01295	SN74LS02N	3	1	
U12	I.C., TTL, Dig, Pos-AND Gates, Totem Pole Outputs Quad 2-Input	393066	01295	SN74LS08N	1	1	
U16	I.C., TTL, Dig, Low-Power Schottky, Dual, J-K, Neg-edge Flip-Flop	414029	01295	SN74LS112N	1	1	
U18	I.C., TTL, Dig, Low-Power, Schottky, Dual D	393124	01295	SN74LS74N	1	1	
U20	I.C., TTL, Quad 2-Input	393033	01295	SN74LS00N	1		
U21	I.C., TTL, Dig, Quad 2-in, Pos-OR Gate w/TP Outputs	393108	01295	SN74LS32N	1	1	

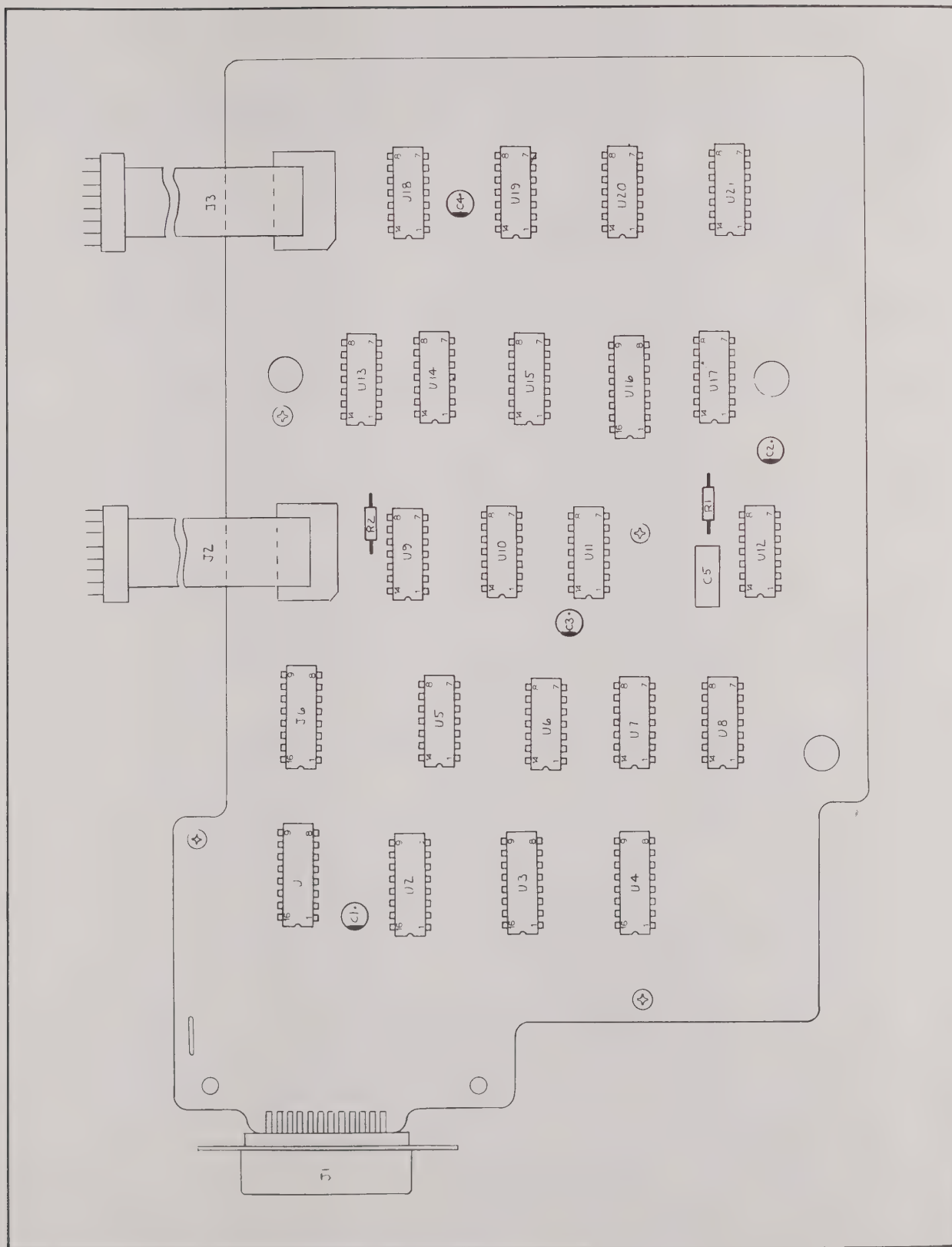


Figure 615-6. IEEE 488 Bus Interface PCB Assy

Table 615-13. Processor PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
IEEE-488 I/F Option—15 Processor PCB Figure 615-7							
C1 thru C4	Cap, Elect, 10 uF, + 50/-10, 25V	170266	73445	ET100X25A2	4	1	
C5	Cap, Taut, 0.47 uF, $\pm$ 20%, 250V	184366	73445	C280AEP470K	1		
C6, C7	Cap, Mica, 22 pF $\pm$ 5%, 500V	148551	72136	DM15C220J	2		
C8, C9	Cap, Taut, 1 uF $\pm$ 20%, 35V	161919	56289	196D105X0035 JA1	2		
C10, C11	Cap, Mica, 100 pF, $\pm$ 5%, 500V	148494	72136	DM15F101J	2		
C12, C13	Cap, fxd, polyester, 0.010 uF $\pm$ 10%, 250V	325548	73445	C280MAEA10K	2		
C14 thru C18	Cap, Taut, 0.22 uF $\pm$ 20%, 35V	161331	56289	196D224X0035 HA1	5		
C19, C23, C24	Cap, Taut, 5.6 uF $\pm$ 20%, 25V	368969	56289	196D565X0025 KA1	3		
C20, C21	Cap, Taut, 10 uF $\pm$ 20%, 35V	417683	56289	196D106X0035 PE4	2		
CR1, CR2, CR3	Diode, si, Hi-Speed 75V, 150MA	203323	07910	1N4448	3	REF	
CR4	Diode, Zener	260695	07910	1N754A	1	1	
J1, J2, J3 J5	Cable	380576	08261	5122-003.5	4		
J4, J6	Socket, I.C.	370304	01295	C931402	2		
L1, L2, L3	Choke, 6 turn	320911	89536	320911	3		
R1	Res, fxd, comp, 51 $\pm$ 5%, $\frac{1}{4}$ W	221879	01121	CB5105	1		
R2	Res, fxd, comp, 680K $\pm$ 5%, $\frac{1}{4}$ W	188433	01121	CB6815	1		
R3,	Res, fxd, comp, 100, $\pm$ 5%, $\frac{1}{4}$ W	147926	01121	CB1015	1		
R4	Res, fxd, comp, 20K $\pm$ 5%, $\frac{1}{4}$ W	221614	01121	CB2035	1		
R5	Res, fxd, comp, 3K $\pm$ 5%, $\frac{1}{4}$ W	193508	01121	CB3025	1		
R6	Res, net, 10K	414003	89536	414003	1		
R7, R8, R9, R10	Res, fxd, comp, 5.6K, $\pm$ 5%, $\frac{1}{4}$ W	148080	01121	CB5625	4		
R11, R12, R17, R19	Res, fxd, MF, 5.11K $\pm$ 1% 1/8W	294868	91637	MFFI-85111F	4		
R13, R20	Res, fxd, MF, 562 $\pm$ 1%, 1/8W	340828	91637	MFFI-85620F	2		

Table 615-13. Processor PCB Assembly (Continued)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R14, R21	Res, fxd, MF, 66.5K $\pm$ 1%, 1/8W	289082	91637	MFF1-86652F	2		
R15, R18	Res, fxd, MF, 549 $\pm$ 1%, 1/8W	436469	91637	MFF1-85490F	2		
R16, R22	Res, Var, 10K $\pm$ 10%, 1/2W	309674	11236	360T103A	2		
R23	Res, fxd, comp, 10K $\pm$ 5%, 1/4W	148106	01121	CB1035	1		
U1, U7	I.C., TTL, Dig, 4-B & Bistable latches	408377	01295	SN74LS75N	2		
U2	I.C., TTL, Dig, Hex Inverter	393058	01295	SN74LS04N	1		
U3, U5	I.C., Dig, 8-Bit, Multiplying, Dig-to Analog Converter	419226	06665	DAC08CZ	2		
U4, U6	I.C., Linear, Op.-Amp	363515	12040	LM301AN	2	1	
U8, U13, U18, U24	I.C., TTL, Dig, Data Selector	407577	01295	SN74LS251	4	1	
U9, U10, U14, U15	I.C., TTL, Dig, 8-Bit Addressable Latch	419242	01295	SN74LS259N	4	1	
U11, U12	I.C., C-MOS, Triple 2 Channel Multiplexer 	375808	95303	CD4053AE	2	1	
U16	I.C., TTL, Dig, Quad 2-in, Pos-OR Gate	393108	01295	SN74LS32N	1	REF	
U17	I.C., Dig, Standard Memory, Interface  	404434	34649	P4289	1	1	
U19	I.C., TTL, Quad, 2-Input	393033	01295	SN74LS00N	1	1	
U20	I.C., TTL, Decoder	407585	01295	SN74LS138N	1	1	
U21, U29	I.C., TTL, Dig, Dual, J-K Neg-edge Triggered Flip-Flop	393157	01295	SN74LS107N	2	1	
U22	I.C., Dig, Central Processor Unit  	404418	34649	C4040	1	1	
U23	I.C., Dig, Bit ROM  	418129	34649	C2708	1	1	
U25, U26	I.C., TTL, Dig, BCD to Decimal Decoder Driver	419192	01295	SN74LS145N	2	1	
U27	I.C., TTL, Triple, 3-Input Pos-NOR Gate	393090	01295	SN74LS27N	1	1	
U28	I.C., Clock Generator, Micro-Computer Set 	404459	34649	C4201	1	1	
U30	I.C., Dig, C-MOS Hand Gates Quad, 2-Input 	355198	04713	MC14011CP	1	1	
U31	I.C., Dig, TTL, COS-MOS, 8-Input NOR Gate 	408781	95303	CD4078B	1	1	
U32	I.C., TTL, Dig, tri-state buffer	429902	12040	DM81L595N	1	1	
XU17	Socket, I.C., 40 pin	376244	01295	C934002	1		
XU22, XU23	Socket, I.C., 24 pin  Indicates MOS device which may be damaged by static discharge	376236	01295	C932402	2		

Table 615-13. Processor PCB Assembly (Concluded)

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
Y1	Crystal, 5.185 MHz  These items are not installed in the PCB Assembly if ordered using P/N 440222. They must be ordered separately if they are required.	408518	89536	408518	1		

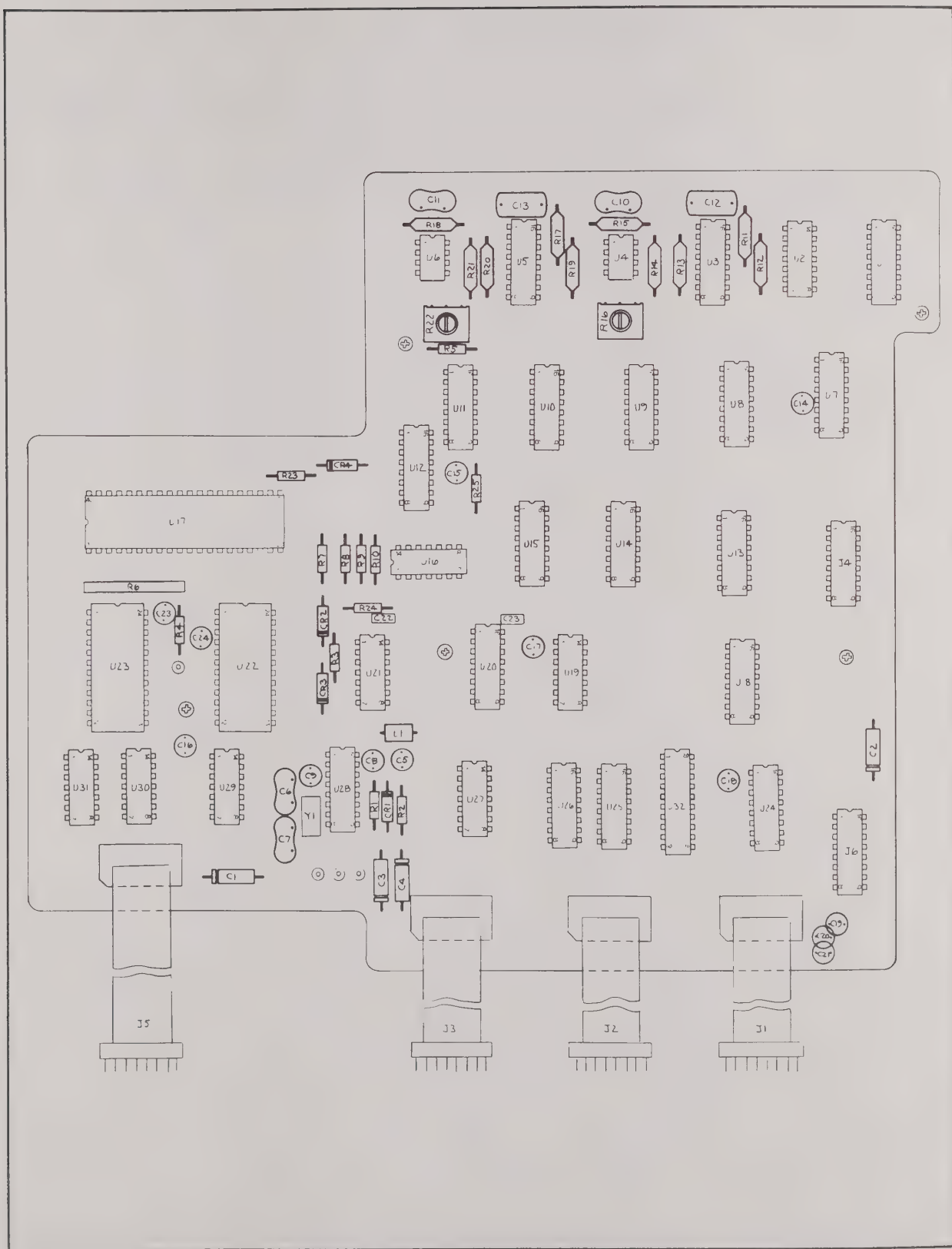


Figure 615-7. IEEE 488 Processor PCB Assy

615-22

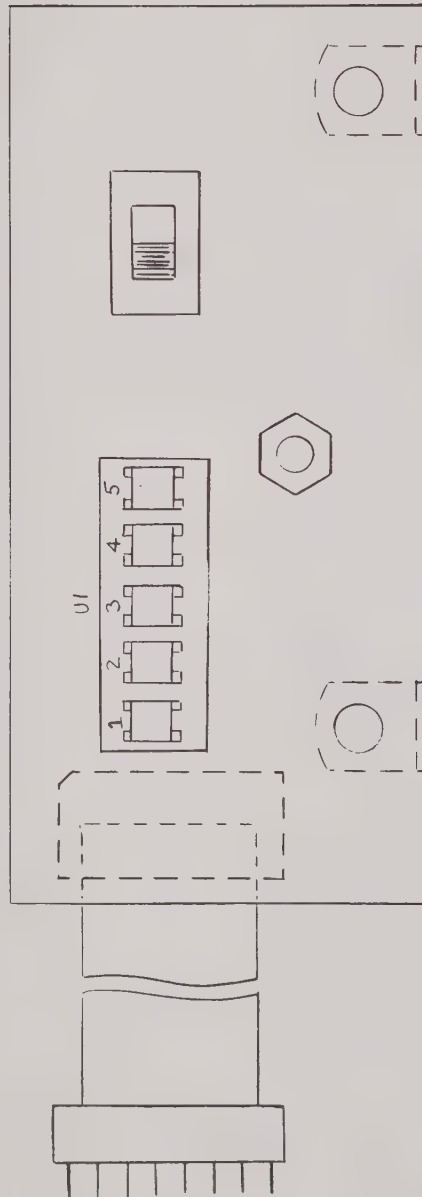


Figure 615-8. IEEE 488 Switchboard PCB Assy

Option —16 Rear Panel Inputs

The 1953A can be ordered with three factory-installed BNC connectors on the rear panel which serve as inputs to channels A, B and C. When this option is ordered, no front panel connector is installed for the channel C input. The channels A and B inputs are in parallel with the corresponding front panel inputs. The addition of the rear panel input terminals for channels A and B increases the input capacity of these channels to 85 pF.

NOTE

Sensitivity on the A Channel is reduced to 30 mV at 75 MHz, decreasing to 100 mV at 125 MHz, as measured from the rear connector. When using the rear "A" connector at frequencies above 75 MHz a 50 ohm termination is recommended at the front "A" connector to reduce effects of standing waves.

Table 616-1. Rear Inputs

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	REAR INPUTS Option —16						
	Coax Cable Assy (channel A)	433383	89536	433383	1		
	Coax Cable Assy (channel B)	433391	89536	433391	1		
	Connector, BNC	152033	95712	30355-1	2		
	Cable Assy (channel C)	406934	89536	406934	1		

Option —20

Superior Oven-Stabilized Timebase

620-1. Introduction

620-2. The Superior Ovenized Oscillator affords the highest degree of timebase stability available to the Model 1953A. The specifications for Option —20 are given in Section 1. The unit is installed on the inside of the rear panel of the 1953A, and requires re-arrangement of the instrument's power switching. A switch installed on the rear panel of the 1953A is used to activate the heaters independently of the power switch for the instrument itself. The option must be ordered factory-installed in the 1953A when the instrument is purchased, it is not field-installable.

620-3. Calibration

620-4. Calibration of the Ovenized Oscillator is similar to that of the other timebases. Proceed as follows:

- a. Connect 1953A to ac line power.
- b. Turn CYCLE RATE control cw, off the OFF detent.
- c. Set FUNCTION switch to FREQ A.
- d. Set CONT/TRIG switch to TRIG.
- e. Connect 10 MHz frequency standard to CHANNEL A connector.
- f. Adjust channel A TRIGGER LEVEL control to establish proper input signal triggering.
- g. Set RANGE switch to 10s (GATE 4).
- h. Momentarily press RESET button. After 10 seconds 1953A display should indicate: 10000.0000 kHz.
- i. If display is incorrect locate the adjustment screw access hole on the rear panel. Using an insulated tuning tool, turn the adjustment slightly.
- j. Momentarily press RESET button. Observe the display for a change in the readout.
- k. Repeat steps h, i and j until the display reads 10000.0000 kHz.

Table 620-1. Superior Oven-Stabilized Timebase

REF DESIG OR ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG FED SPLY CDE	MFG PART. NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	SUPERIOR OVEN-STABILIZED TIMEBASE Option -20						
	<i>NOTE</i> <i>Unless otherwise noted components are installed on the Main pcb. Refer to Figure 5-5.</i>						
C91	Cap, elect, 4000 uF -10/+100%, 25V	370742	99392	39C25JJ43	1	1	
C121	Cap, cer, 10,000 pF ±20%, 100V	407361	72982	8121-A100-W5R 103M	1		
C122, C123	Cap, tant, 10 uF ±20%, 35V	417683	56289	196D106X0035 PE4	2		
C124	Cap, mica, 39 pF ±5%, 500V	148544	72136	DM15E390J	1		
R121	Res, var, cer, 10K ±20%, 1/2W	267880	11236	190PC103B	1	1	
R128	Res, comp, 1.8K ±5%, 1/4W	175042	01121	CB1825	1		
S121	Switch, toggle 	327734	09353	7201LHPZG1	1		
U7	Oscillator 	416826	12020	48-65B	1		
U91	Rect, Bridge	296509	09423	FB200	1		
U101	Reg Assy + 18V	443713	89536	443713	1		
	Cable Assy	443721	89536	443721	1		
	Decal 	428052	89536	428052	1		
	Attached to rear panel						
	Attached to inside right chassis of instrument						
	Attached to front panel - power switch						

Section 7

General Information

7-1. This section of the manual contains generalized user information as well as supplemental information to the List of Replaceable parts contained in Section 5. The following information is presented in this section:

List of Abbreviations

Federal Supply Codes for Manufacturers

Fluke Technical Service Centers — U.S. and Canada

Sales and Service Locations — International

Sales Representatives — U.S. and Canada

List of Abbreviations and Symbols

A or amp	ampere	H	henry	pF	picofarad
ac	alternating current	hd	heavy duty	pn	part number
af	audio frequency	hf	high frequency	(+) or pos	positive
a/d	analog-to-digital	Hz	hertz	pot	potentiometer
assy	assembly	IC	integrated circuit	p-p	peak-to-peak
AWG	american wire gauge	if	intermediate frequency	ppm	parts per million
B	bel	in	inch(es)	PROM	programmable read-only memory
bcd	binary coded decimal	intl	internal	psi	pound-force per square inch
°C	Celsius	I/O	input/output	RAM	random-access memory
cap	capacitor	k	kilo (10^3)	rf	radio frequency
ccw	counterclockwise	kHz	kilohertz	rms	root mean square
cer	ceramic	k Ω	kilohm(s)	ROM	read-only memory
cermet	ceramic to metal(seal)	kV	kilovolt(s)	s or sec	second (time)
ckt	circuit	lf	low frequency	scope	oscilloscope
cm	centimeter	LED	light-emitting diode	SH	shield
cmrr	common mode rejection ratio	LSB	least significant bit	Si	silicon
comp	composition	LSD	least significant digit	serno	serial number
cont	continue	M	mega (10^6)	sr	shift register
crt	cathode-ray tube	m	milli (10^{-3})	Ta	tantalum
cw	clockwise	mA	milliampere(s)	tb	terminal board
d/a	digital-to-analog	max	maximum	tc	temperature coefficient or temperature compensating
dac	digital-to-analog converter	mf	metal film	tcxo	temperature compensated crystal oscillator
dB	decibel	MHz	megahertz	tp	test point
dc	direct current	min	minimum	u or μ	micro (10^{-6})
dmm	digital multimeter	mm	millimeter	uhf	ultra high frequency
dvm	digital voltmeter	ms	millisecond	us or μ s	microsecond(s) (10^{-6})
elect	electrolytic	MSB	most significant bit	uut	unit under test
ext	external	MSD	most significant digit	V	volt
F	farad	MTBF	mean time between failures	v	voltage
°F	Fahrenheit	MTTR	mean time to repair	var	variable
FET	Field-effect transistor	mV	millivolt(s)	vco	voltage controlled oscillator
ff	flip-flop	mv	multivibrator	vhf	very high frequency
freq	frequency	M Ω	megohm(s)	vlf	very low frequency
FSN	federal stock number	n	nano (10^{-9})	W	watt(s)
g	gram	na	not applicable	ww	wire wound
G	giga (10^9)	NC	normally closed	xfmr	transformer
gd	guard	(-) or neg	negative	xstr	transistor
Ge	germanium	NO	normally open	xtal	crystal
GHz	gigahertz	ns	nanosecond	xtlo	crystal oscillator
gmV	guaranteed minimum value	opnl ampl	operational amplifier	Ω	ohm(s)
gnd	ground	p	pico (10^{-12})	μ	micro (10^{-6})
		para	paragraph		
		pcb	printed circuit board		

Federal Supply Codes for Manufacturers (Continued)

00213 Nytronics Comp. Group Inc. Subsidiary of Nytronics Inc. Formerly Sage Electronics Rochester, New York	03797 Eldema Div. Genisco Technology Corp. Compton, California	05574 Viking Industries Chatsworth, California	07597 Burndy Corp. Tape/Cable Div. Rochester, New York
00327 Welwyn International, Inc. Westlake, Ohio	03877 Transistron Electronic Corp. Wakefield, Massachusetts	05704 Replaced by 16258	07792 Lerma Engineering Corp. Northampton, Massachusetts
00656 Aerovox Corp. New Bedford, Massachusetts	03888 KDI Pyrofilm Corp. Whippany, New Jersey	05820 Wakefield Engineering Inc. Wakefield, Massachusetts	07910 Teledyne Semiconductor Formerly Continental Device Hawthorne, California
00686 Film Capacitors, Inc. Passaic, New Jersey	03911 Clairex Electronics Div. Clairex Corp. Mt. Vernon, New York	06001 General Electric Co. Electronic Capacitor & Battery Products Dept. Columbia, South Carolina	07933 - use 49956 Raytheon Co. Semiconductor Div. HQ Mountain View, California
00779 AMP Inc. Harrisberg, Pennsylvania	03980 Muirhead Inc. Mountainside, New Jersey	06136 Replaced by 63743	08225 Industro Transistor Corp. Long Island City, New York
01121 Allen-Bradley Co. Milwaukee, Wisconsin	04009 Arrow Hart Inc. Hartford, Connecticut	06383 Panduit Corp. Tinley Park, Illinois	08261 Spectra Strip Corp. Garden Grove, California
01281 TRW Electronic Corp. Semiconductor Operations Lawndale, California	04062 Replaced by 72136	06473 Bunker Ramo Corp. Amphenol SAMS Div. Chatsworth, California	08530 Reliance Mica Corp. Brooklyn, New York
01295 Texas Instruments, Inc. Semiconductor Group Dallas, Texas	04202 Replaced by 81312	06555 Beede Electrical Instrument Co. Penacook, New Hampshire	08806 General Electric Co. Miniature Lamp Products Dept. Cleveland, Ohio
01537 Motorola Communications & Electronics Inc. Franklin Park, Illinois	04217 Essex International Inc. Wire & Cable Div. Anaheim, California	06739 Electron Corp. Littleton, Colorado	08863 Nylomatic Corp. Norrisville, Pennsylvania
01686 RCL Electronics Inc. Manchester, New Hampshire	04221 Aemco, Div. of Midtex Inc. Mankato, Minnesota	06743 Clevite Corp. Cleveland, Ohio	08988 - use 53085 Skottie Electronics Inc. Archbald, Pennsylvania
01730 Replaced by 73586	04222 AVX Ceramics Div. AVX Corp. Myrtle Beach, Florida	06751 Components, Inc. Semcor Div. Phoenix, Arizona	09214 G.E. Co. Semi-Conductor Products Dept. Power Semi-Conductor Products OPN Sec. Auburn, New York
01884 - use 56289 Sprague Electric Co. Dearborn Electronic Div. Lockwood, Florida	04423 Telonic Industries Laguna Beach, California	06860 Gould Automotive Div. City of Industry, California	09353 C and K Components Watertown, Massachusetts
02114 Ferroxcube Corp. Saugerties, New York	04645 Replaced by 75376	06961 Vernitron Corp., Piezo Electric Div. Formerly Clevite Corp., Piezo Electric Div. Bedford, Ohio	09423 Scientific Components, Inc. Santa Barbara, California
02131 General Instrument Corp. Harris ASW Div. Westwood, Maine	04713 Motorola Inc. Semiconductor Products Phoenix, Arizona	06980 Eimac Div. Varian Associates San Carlos, California	09922 Burndy Corp. Norwalk, Connecticut
02395 Rason Mfg. Co. Brooklyn, New York	04946 Standard Wire & Cable Los Angeles, California	07047 Ross Milton, Co., The South Hampton, Pennsylvania	09969 Dale Electronics Inc. Yankton, S. Dakota
02533 Snelgrove, C.R. Co., Ltd. Don Mills, Ontario, Canada M3B 1M2	05082 Replaced by 94988	07115 Replaced by 14674	10059 Barker Engineering Corp. Formerly Amerace, Amerace ESNA Corp. Kenilworth, New Jersey
02606 Fenwal Labs Div. of Travenel Labs. Morton Grove, Illinois	05236 Jonathan Mfg. Co. Fullerton, California	07138 Westinghouse Electric Corp., Electronic Tube Division Horsehead, New York	11236 CTS of Berne Berne, Indiana
02660 Bunker Ramo Corp., Conn Div. Formerly Amphenol-Borg Electric Corp. Broadview, Illinois	05245 Components Corp. now Corcom, Inc. Chicago, Illinois	07233 TRW Electronic Components Cinch Graphic City of Industry, California	11237 CTS Keene Inc. Paso Robles, California
02799 Areo Capacitors, Inc. Chatsworth, California	05277 Westinghouse Electric Corp. Semiconductor Div. Youngwood, Pennsylvania	07256 Silicon Transistor Corp. Div. of BBF Group Inc. Chelmsford, MA	11358 CBS Electronic Div. Columbia Broadcasting System Newburyport, MN
03508 General Electric Co. Semiconductor Products Syracuse, New York	05278 Replaced by 43543	07261 Aumet Corp. Culver City, California	11403 Best Products Co. Chicago, Illinois
03614 Replaced by 71400	05279 Southwest Machine & Plastic Co. Glendora, California	07263 Fairchild Semiconductor Div. of Fairchild Camera & Instrument Corp. Mountain View, California	11503 Keystone Columbia Inc. Warren, Michigan
03651 Replaced by 44655	05397 Union Carbide Corp. Materials Systems Div. New York, New York	07344 Bircher Co., Inc. Rochester, New York	11532 Teledyne Relays Hawthorne, California

Federal Supply Codes for Manufacturers (Continued)

11711 General Instrument Corp Rectifier Division Hickville, New York	14099 Semtech Corp. Newbury Park, California	17069 Circuit Structures Lab. Burbank, California	24655 General Radio Concord, Massachusetts
11726 Qualidyne Corp. Santa Clara, California	14140 Edison Electronic Div. Mc Gray-Edison Co. Manchester, New Hampshire	17338 High Pressure Eng. Co., Inc. Oklahoma City, Oklahoma	24759 Lenox-Fugle Electronics Inc. South Plainfield, New Jersey
12014 Chicago Rivet & Machine Co. Bellwood, Illinois	14193 Cal-R-Inc. formerly California Resistor, Corp. Santa Monica, California	17545 Atlantic Semiconductors, Inc. Asbury Park, New Jersey	25088 Siemen Corp. Isilen, New Jersey
12040 National Semiconductor Corp. Danbury, Connecticut	14298 American Components, Inc. an Insilco Co. Conshohocken, Pennsylvania	17856 Siliconix, Inc. Santa Clara, California	25403 Amperex Electronic Corp. Semiconductor & Micro-Circuits Div. Slatersville, Rhode Island
12060 Diodes, Inc. Chatsworth, California	14655 Cornell-Dublier Electronics Division of Federal Pacific Electric Co. Govt. Control Dept. Newark, New Jersey	17870 Replaced by 14140	27014 National Semiconductor Corp. Santa Clara, California
12136 Philadelphia Handle Co. Camden, New Jersey	14752 Electro Cube Inc. San Gabriel, California	18178 Vactec Inc. Maryland Heights, Missouri	27264 Molex Products Downers Grove, Illinois
12300 Potter-Brumfield Division AMF Canada LTD. Guelph, Onatrio, Canada	14869 Replaced by 96853	18324 Signetics Corp. Sunnyvale, California	28213 Minnesota Mining & Mfg. Co. Consumer Products Div. St. Paul, Minnesota
12323 Presin Co., Inc. Shelton, Connecticut	14936 General Instrument Corp. Semi Conductor Products Group Hicksville, New York	18612 Vishay Resistor Products Div. Vishay Intertechnology Inc. Malvern, Pennsylvania	28425 Serv.-/Link formerly Bohannon Industries Fort Worth, Texas
12327 Freeway Corp. formerly Freeway Washer & Stamping Co. Cleveland, Ohio	15636 Elec-Trol Inc. Saugus, California	18736 Voltronics Corp. Hanover, New Jersey	28478 Deltrol Controls Div. Deltrol Corporation Milwaukee, Wisconsin
12443 Budd Co. The, Polychem Products Plastic Products Div. Bridgeport, PA	15801 Fenwal Electronics Inc. Div. of Kidde Walter and Co., Inc. Framingham, Massachusetts	18927 G T E Sylvania Inc. Precision Material Group Parts Division Titusville, Pennsylvania	28480 Hewlett Packard Co. Corporate H.Q. Palo Alto, California
12615 U.S. Terminals Inc. Cincinnati, Ohio	15818 Teledyne Semiconductors, formerly Amelco Semiconductor Mountain View, California	19451 Perine Machinery & Supply Co. Seattle, Washington	28520 Heyman Mfg. Co. Kenilworth, New Jersey
12617 Hamlin Inc. Lake Mills, Wisconsin	15849 Litton Systems Inc. Useco Div. formerly Useco Inc. Van Nuys, California	19701 Electro-Midland Corp. Mepco-Electra Inc. Mineral Wells, Texas	29083 Monsanto, Co., Inc. Santa Clara, California
12697 Clarostat Mfg. Co. Dover, New Hampshire	15898 International Business Machines Corp. Essex Junction, Vermont	20584 Enochs Mfg. Inc. Indianapolis, Indiana	29604 Stackpole Components Co. Raleigh, North Carolina
12749 James Electronics Chicago, Illinois	15909 Replaced by 14140	20891 Self-Organizing Systems, Inc. Dallas, Texas	30148 A B Enterprise Inc. Ahoskie, North Carolina
12856 Micrometals Sierra Madre, California	16258 Space-Lok Inc. Burbank, California	21604 Buckeye Stamping Co. Columbus, Ohio	30323 Illinois Tool Works, Inc. Chicago, Illinois
12954 Dickson Electronics Corp. Scottsdale, Arizona	16299 Corning Glass Electronic Components Div. Raleigh, North Carolina	21845 Solitron Devices Inc. Transistor Division Riveria Beach, Florida	31091 Optimax Inc. Colmar, Pennsylvania
12969 Unitrode Corp. Watertown, Massachusetts	16332 Replaced by 28478	22767 ITT Semiconductors Palo Alto, California	32539 Mura Corp. Great Neck, New York
13103 Thermalloy Co., Inc. Dallas, Texas	16473 Cambridge Scientific Ind. Div. of Chemed Corporation Cambridge, Maryland	23050 Product Comp. Corp. Mount Vernon, New York	32767 Griffith Plastic Corp. Burlingame, California
13327 Solitron Devices Inc. Tappan, New York	16742 Paramount Plastics Fabricators, Inc. Downey, California	23732 Tracor Inc. Rockville, Maryland	32879 Advanced Mechanical Components Northridge, California
13511 Amphenol Cadre Div. Bunker-Ramo Corp. Los Gatos, California	16758 Delco Electronics Div. of General Motors Corp. Kokomo, Indiana	23880 Stanford Applied Engrng. Santa Clara, California	32897 Erie Technological Products, Inc. Frequency Control Div. Carlisle, Pennsylvania
13606 - use 56289 Sprague Electric Co. Transistor Div. Concord, New Hampshire	17001 Replaced by 71468	23936 Pamotor Div., Wm. J. Purdy Co. Burlingame, California	32997 Bourns Inc. Trimpot Products Division Riverside, California
13839 Replaced by 23732		24248 Replaced by 94222	33173 General Electric Co. Products Dept. Owensboro, Kentucky
		24355 Analog Devices Inc. Norwood, Massachusetts	

Federal Supply Codes for Manufacturers (Continued)

34333 Silicon General Westminister, California	70563 Amperite Company Union City, New Jersey	73293 Hughes Aircraft Co. Electron Dynamics Div. Torrence, California	77969 Rubbercraft Corp. of CA. LTD. Torrance, California
34335 Advanced Micro Devices Sunnyvale, California	70903 Belden Corp. Geneva, Illinois	73445 Amperex Electronic Corp. Hicksville, LI, New York	78189 Shakeproof Div. of Illinois Tool Works Inc. Elgin, Illinois
34802 Electromotive Inc. Kenilworth, New Jersey	71002 Birnbach Radio Co., Inc. Freeport, LI New York	73559 Carling Electric Inc. West Hartford, Connecticut	78277 Sigma Instruments, Inc. South Braintree, Massachusetts
37942 Mallory, P.R. & Co., Inc. Indianapolis, Indiana	71400 Bussmann Mfg. Div. of McGraw-Edison Co. Saint Louis, Missouri	73586 Circle F Industries Trenton, New Jersey	78488 Stackpole Carbon Co. Saint Marys, Pennsylvania
42498 National Radio Melrose, Massachusetts	71450 CTS Corp. Elkhart, Indiana	73734 Federal Screw Products, Inc. Chicago, Illinois	78553 Eaton Corp. Engineered Fastener Div. Tinnerman Plant Cleveland, Ohio
43543 Nytronics Inc. Transformer Co. Div. Geneva, New York	71468 ITT Cannon Electric Inc. Santa Ana, California	73743 Fischer Special Mfg. Co. Cincinnati, Ohio	79136 Waldes Kohinoor Inc. Long Island City, New York
44655 Ohmite Mfg. Co. Skokie, Illinois	71482 Clare, C.P. & Co. Chicago, Illinois	73899 JFD Electronics Co. Components Corp Brooklyn, New York	79497 Western Rubber Company Goshen, Indiana
49671 RCA Corp. New York, New York	71590 Centrelab Electronics Div. of Globe Union Inc. Milwaukee, Wisconsin	73949 Guardian Electric Mfg. Co. Chicago, Illinois	79963 Zierick Mfg. Corp. Mt. Kisko, New York
49956 Raytheon Company Lexington, Massachusetts	71707 Coto Coil Co., Inc. Providence, Rhode Island	74199 Quan Nichols Co. Chicago, Illinois	80031 Electro-Midland Corp., Mepco Div. A North American Phillips Co. Morristown, New Jersey
50088 Mostek Corp. Carrollton, Texas	71744 Chicago Miniature Lamp Works Chicago, Illinois	74217 Radio Switch Corp. Marlboro, New Jersey	80145 LFE Corp., Process Control Div. formerly API Instrument Co. Chesterland, Ohio
50579 Litronix Inc. Cupertino, California	71785 TRW Electronics Components Cinch Connector Operations Div. Elk Grove Village, Chicago, Illinois	74276 Signalite Div. General Instrument Corp. Neptune, New Jersey	80183 - use 56289 Sprague Products North Adams, Massachusetts
51605 Scientific Components Inc. Linden, New Jersey	72005 Driver, Wilber B., Co. Newark, New Jersey	74306 Piezo Crystal Co. Carlisle, Pennsylvania	80294 Bourns Inc., Instrument Div. Riverside, California
53021 Sangamo Electric Co. Springfield, Illinois	72092 Replaced by 06980	74542 Hoyt Elect. Instr. Works Penacook, New Hampshire	80583 Hammarlund Mfg. Co., Inc. Red Bank, New Jersey
54294 Cutler-Hammer Inc. formerly Shallcross, A Cutter-Hammer Co. Selma, North Carolina	72136 Electro Motive Mfg. Co. Williamamantic, Connecticut	74970 Johnson E.F., Co. Waseca, Minnesota	80640 Stevens, Arnold Inc. South Boston, Massachusetts
55026 Simpson Electric Co. Div. of Am. Gage and Mach. Co. Elgin, Illinois	72259 Nytronics Inc. Pelham Manor, New Jersey	75042 TRW Electronics Components IRC Fixed Resistors Philadelphia, Pennsylvania	81073 Grayhill, Inc. La Grange, Illinois
56289 Sprague Electric Co. North Adams, Massachusetts	72619 Dialight Div. Amperex Electronic Corp. Brooklyn, New York	75376 Kurz-Kasch Inc. Dayton, Ohio	81312 Winchester Electronics Div. of Litton Industries Inc. Oakville, Connecticut
58474 Superior Electric Co. Bristol, Connecticut	72653 G.C. Electronics Div. of Hydrometals, Inc. Brooklyn, New York	75378 CTS Knights Inc. Sandwich, Illinois	81439 Therm-O-Disc Inc. Mansfield, Ohio
60399 Torin Corp, formerly Torrington Mfg. Co. Torrington, Connecticut	72665 Replaced by 90303	75382 Kulka Electric Corp. Mount Vernon, New York	81483 International Rectifier Corp. Los Angeles, California
63743 Ward Leonard Electric Co., Inc. Mount Vernon, New York	72794 Dzus Fastener Co., Inc. West Islip, New York	75915 Littlefuse Inc. Des Plaines, Illinois	81590 Korby Mfg. Co. Seattle, Washington
64834 West Mfg. Co. San Francisco, Californai	72928 Gulton Ind. Inc. Gudeman Div. Chicago, Illinois	76854 Oak Industries Inc. Switch Div. Crystal Lake, Illinois	81741 Chicago Lock Co. Chicago, Illinois
65092 Weston Instruments Inc. Newark, New Jersey	72982 Erie Tech. Products Inc. Erie, Pennsylvania	77342 AMF Inc. Potter & Brumfield Div. Princeton, Indiana	82305 Palmer Electronics Corp. South Gate, California
66150 Winslow Tele-Tronics Inc. Eaton Town, New Jersey	73138 Beckman Instruments Inc. Helipot Division Fullerton, California	77638 General Instrument Corp. Rectifier Division Brooklyn, New York	82389 Switchcraft Inc. Chicago, Illinois
70485 Atlantic India Rubber Works Chicago, Illinois			

Federal Supply Codes for Manufacturers (Concluded)

82415 North American Phillips Controls Corp. Frederick, Maryland	88245 Litton Systems Inc. Usco Div. Van Nuys, California	91934 Miller Electric Co., Inc. Div of Aunet Woonsocket, Rhode Island	97966 Replaced by 11358
82872 Roanwell Corp. New York, New York	88419 Cornell-Dubilier Electronic Div. Federal Pacific Co. Fuquay-Varian, North Carolina	92194 Alpha Wire Corp. Elizabeth, New Jersey	98094 Replaced by 49956
82877 Rotron Inc. Woodstock, New York	88486 Plastic Wire & Cable Jewitt City, Connecticut	93332 Sylvania Electric Products Semiconductor Products Div. Woburn, Massachusetts	98159 Rubber-Teck, Inc. Gardena, California
82879 ITT Royal Electric Div. Pawtucket, Rhode Island	88690 Replaced by 04217	94145 Replaced by 49956	98278 Malco A Microdot Co., Inc. Connector & Cable Div. Pasadena, California
83003 Varo Inc. Garland, Texas	89536 Fluke, John Mfg. Co., Inc. Seattle, Washington	94154 - use 94988 Wagner Electric Corp. Tung-Sol Div. Newark, New Jersey	98291 Sealectro Corp. Mamaroneck, New York
83058 Carr Co., The United Can Div. of TRW Cambridge, Massachusetts	89730 G.E. Co., Newark Lamp Works Newark, New Jersey	94222 Southco Inc. formerly South Chester Corp. Lester, Pennsylvania	98388 Royal Industries Products Div. San Diego, California
83298 Bendix Corp. Electric Power Division Eatontown, New Jersey	90201 Mallory Capacitor Co. Div of P.R. Mallory Co., Inc. Indianapolis, Indiana	95146 Alco Electronic Products Inc. Lawrence, Massachusetts	98743 Replaced by 12749
83330 Smith, Herman H., Inc. Brooklyn, New York	90211 - use 56365 Square D Co. Chicago, Illinois	95263 Leecraft Mfg. Co. Long Island City, New York	98925 Replaced by 14433
83478 Rubbercraft Corp. of America, Inc. West Haven, Connecticut	90215 Best Stamp & Mfg. Co. Kansas City, Missouri	95264 Replaced by 98278	99120 Plastic Capacitors, Inc. Chicago, Illinois
83594 Burroughs Corp. Electronic Components Div. Plainfield, New Jersey	90303 Mallory Battery Co. Div. of Mallory Co., Inc. Tarrytown, New York	95275 Vitramon Inc. Bridgeport, Connecticut	99217 Bell Industries Elect. Comp. Div. formerly Southern Elect. Div. Burbank, California
83740 Union Carbide Corp. Battery Products Div. formerly Consumer Products Div. New York, New York	91094 Essex International Inc. Suglex/IWP Div. Newmarket, New Hampshire	95303 RCA Corp. Receiving Tube Div. Cincinnati, Ohio	99392 STM Oakland, California
84171 Arco Electronics Great Neck, New York	91293 Johanson Mfg. Co. Boonton, New Jersey	95348 Gordo's Corp. Bloomfield, New Jersey	99515 ITT Jennings Monrovia Plant Div. of ITT Jennings formerly Marshall Industries Capacitor Div. Monrovia, California
84411 TRW Electronic Components TRW Capacitors Ogallala, Nebraska	91407 Replaced by 58474	95354 Methode Mfg. Corp. Rolling Meadows, Illinois	99779 - use 29587 Bunker-Ramo Corp. Barnes Div. Landsdowne, Pennsylvania
84613 Fuse Indicator Corp. Rockville, Maryland	91502 Associated Machine Santa Clara, California	95712 Bendix Corp. Electrical Components Div. Microwave Devices Plant Franklin, Indiana	99800 American Precision Industries Inc. Delevan Division East Aurora, New York
84682 Essex International Inc. Industrial Wire Div. Peabody, Massachusetts	91506 Augat Inc. Attleboro, Massachusetts	95987 Weckesser Co. Inc. Chicago, Illinois	99942 Centrelab Semiconductor Centrelab Electronics Div. of Globe-Union Inc. El Monte, California
86577 Precision Metal Products, of Malden Inc. Stoneham, Massachusetts	91637 Dale Electronics Inc. Columbus, Nebraska	96733 San Fernando Electric Mfg. Co. San Fernando, California	Toyo Electronics (R-Ohm Corp.) Irvine, California
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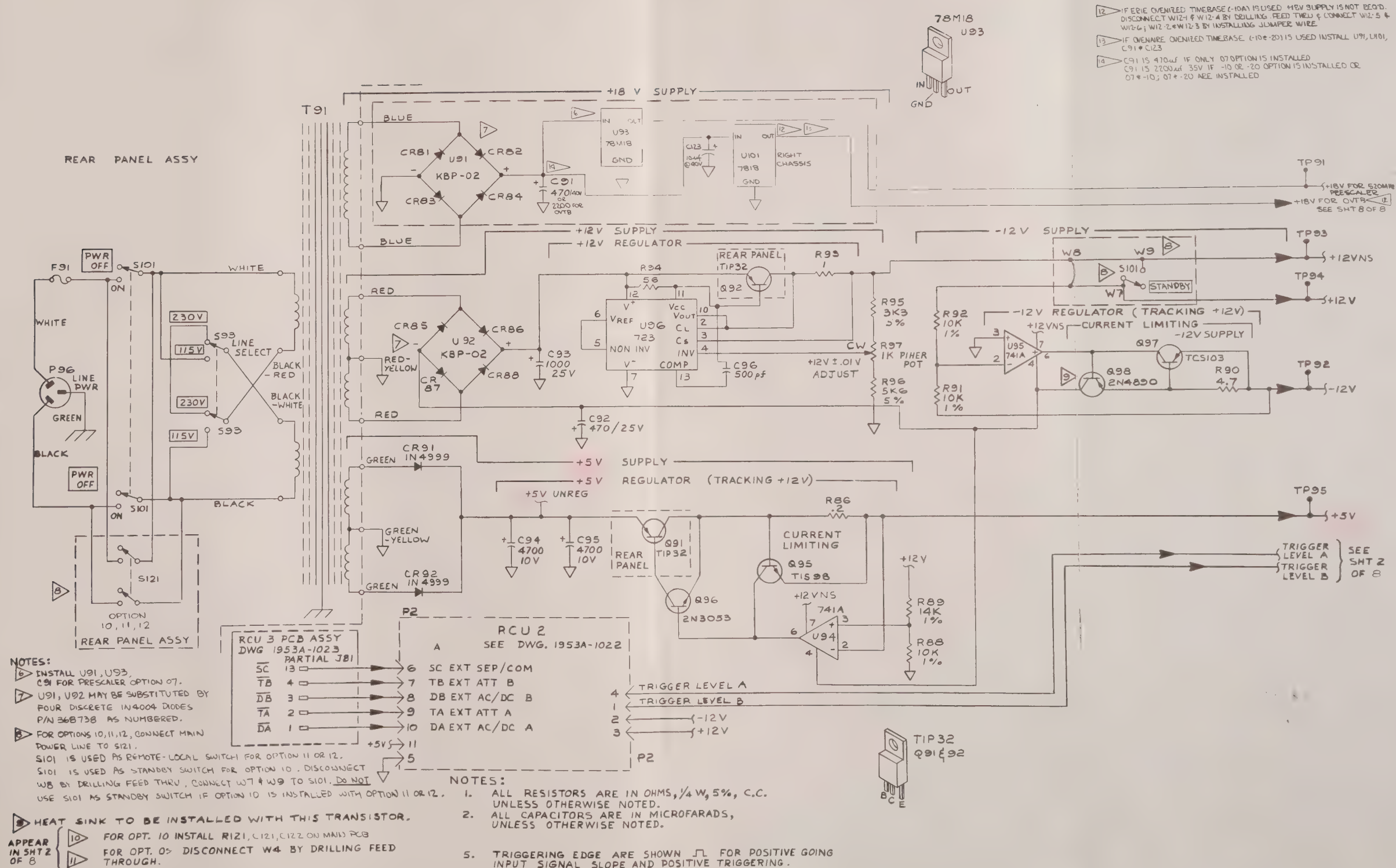
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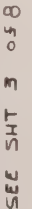
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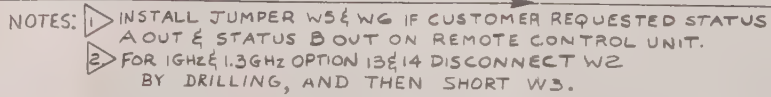
Schematic Diagrams

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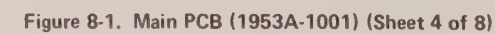


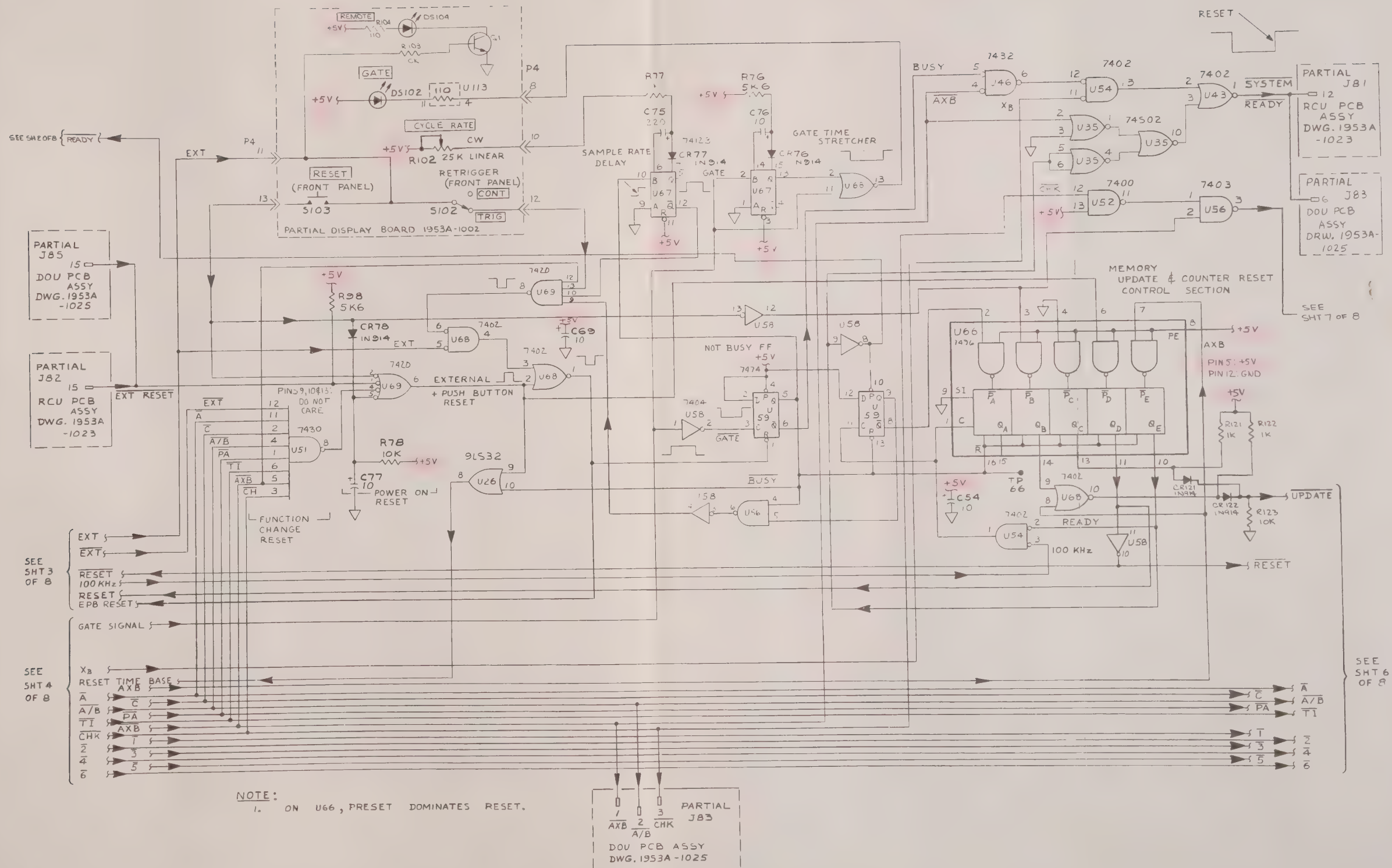


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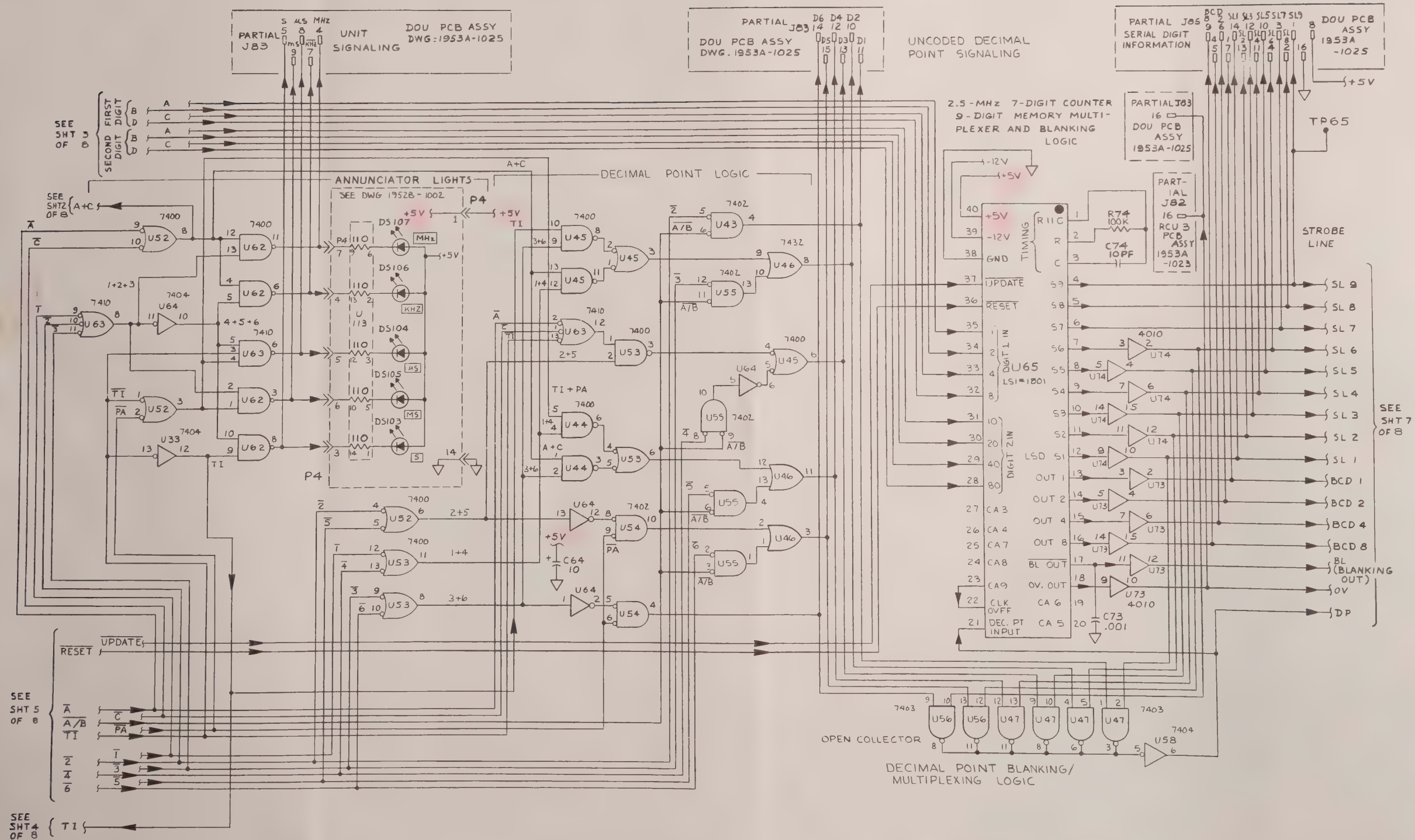


Figure 8-1. Main PCB (1953A-1001) (Sheet 6 of 8)

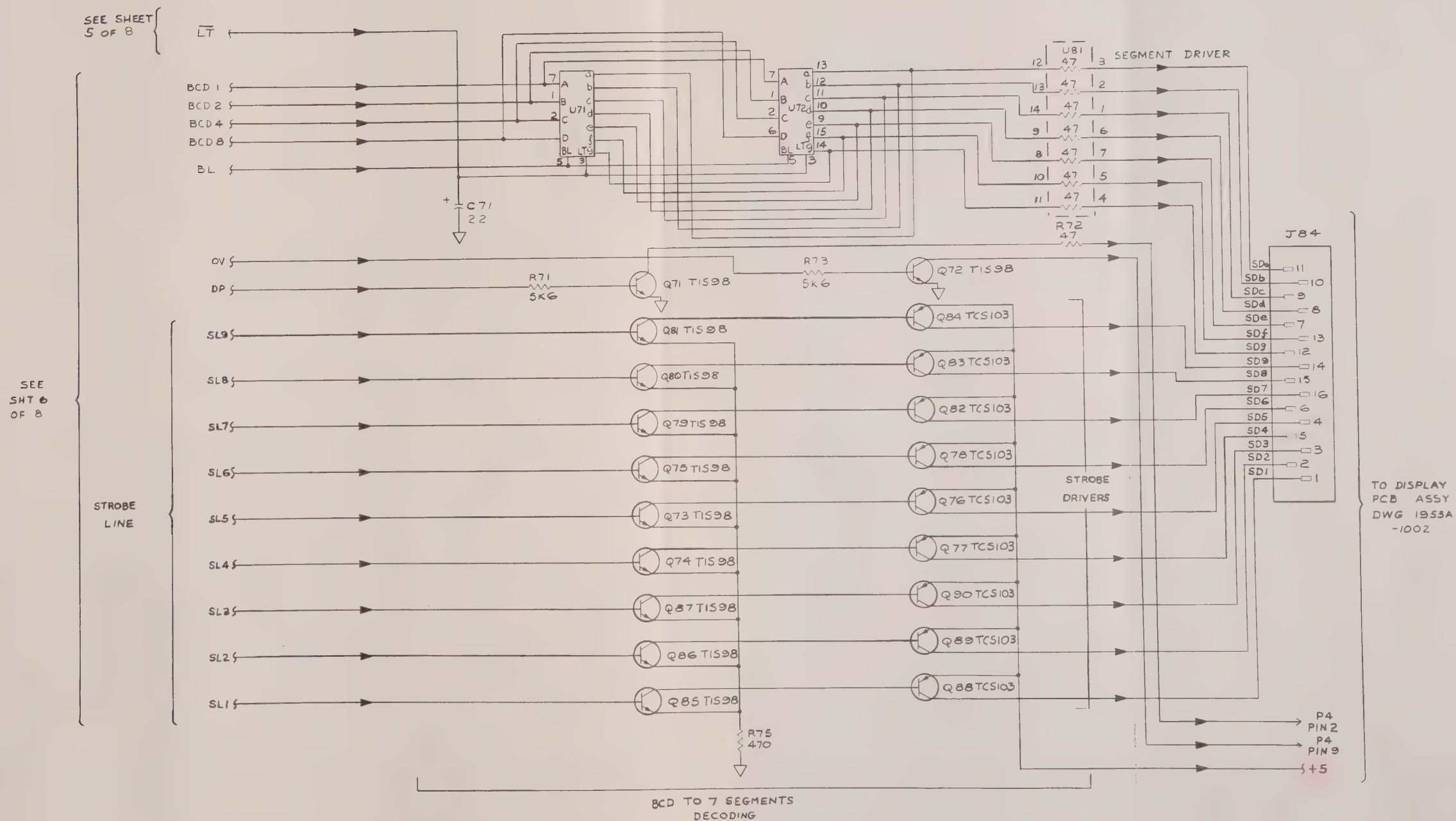


Figure 8-1. Main PCB (1953A-1001) (Sheet 7 of 8)

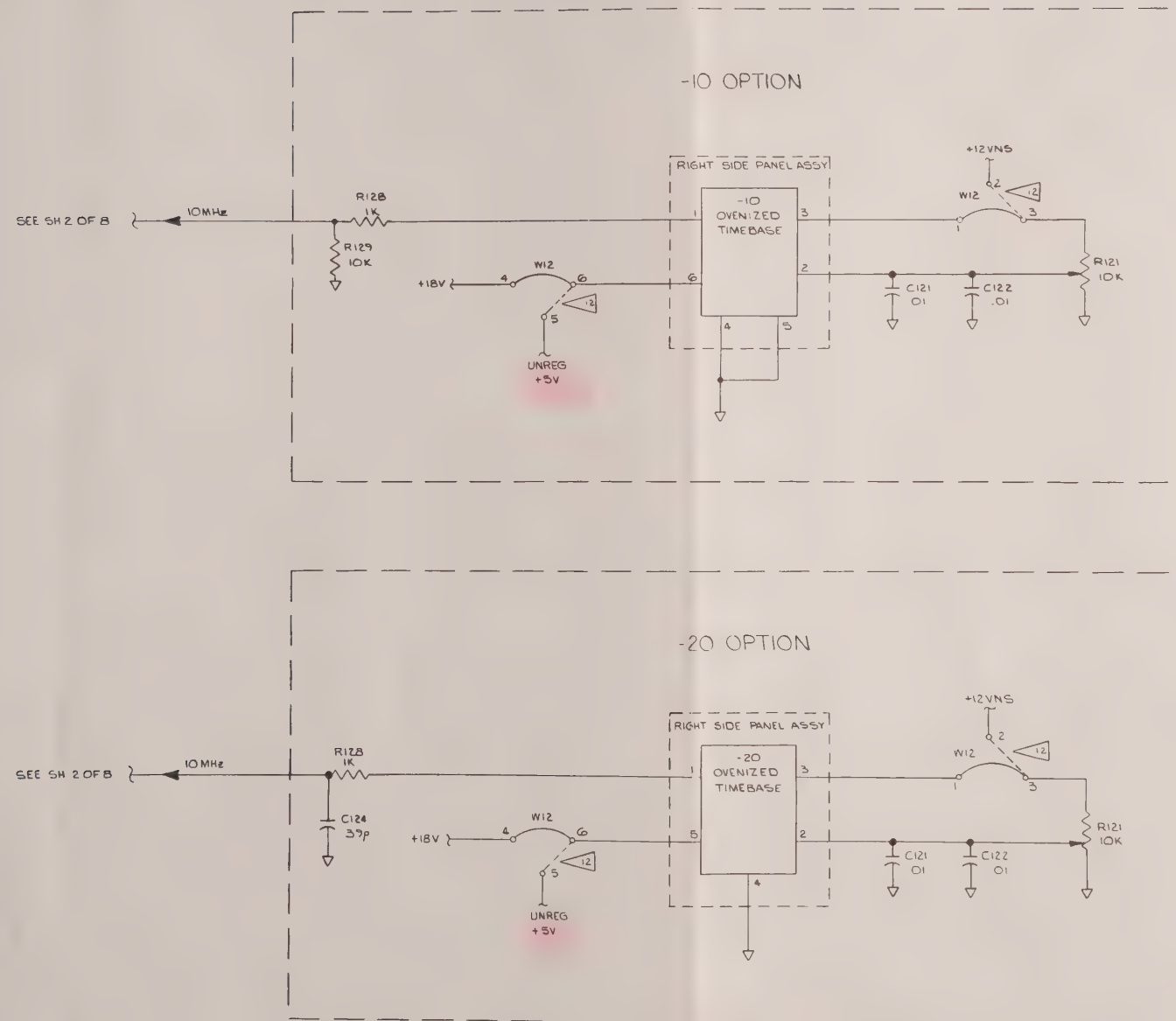
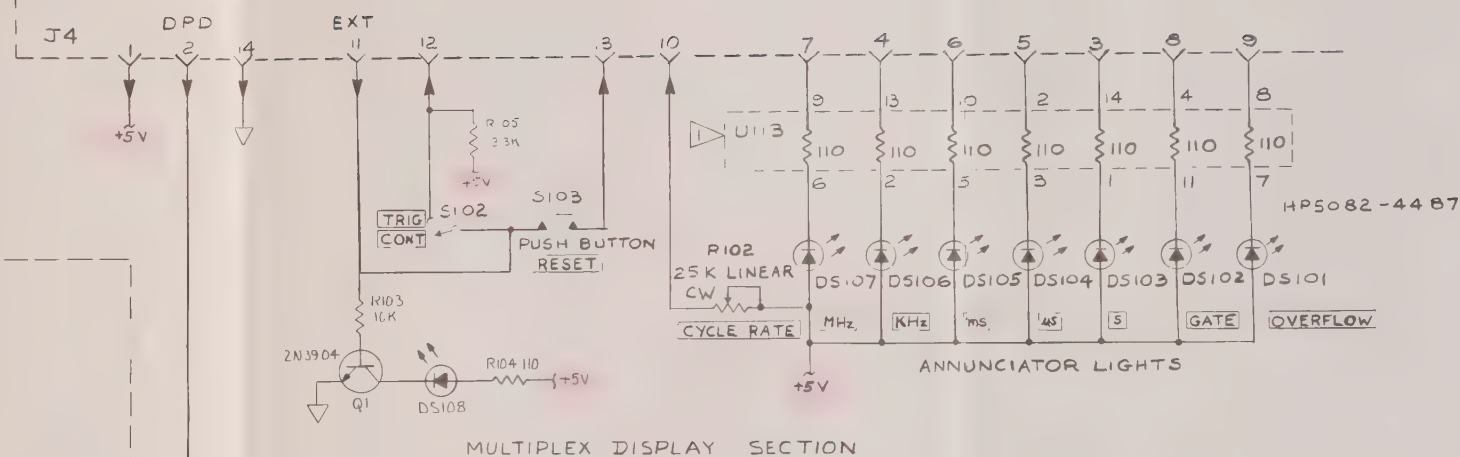
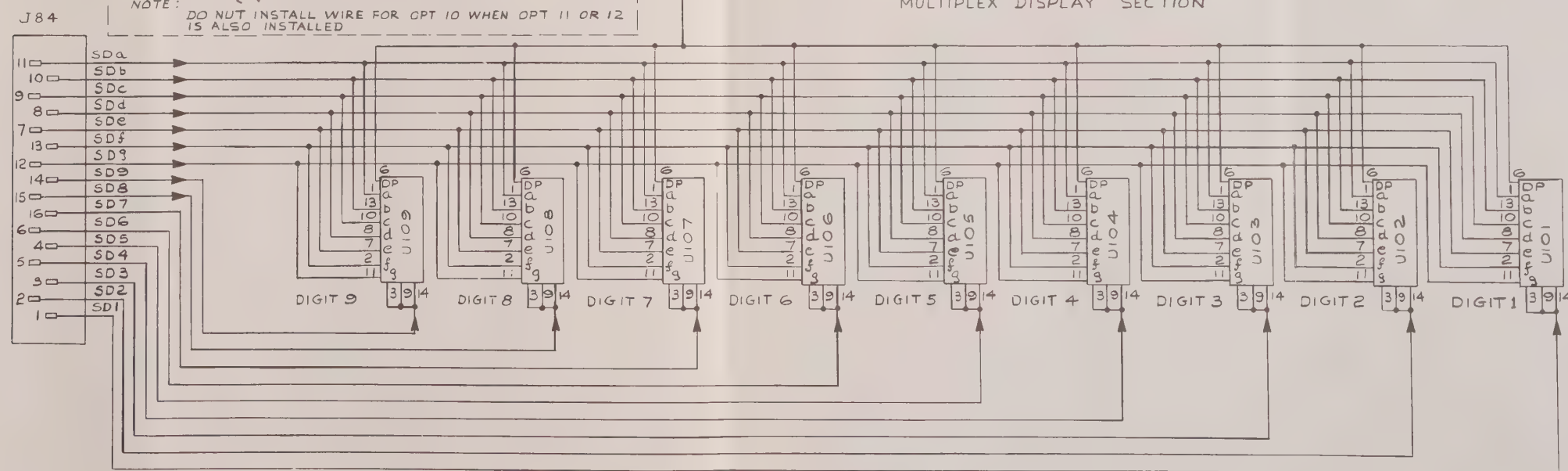
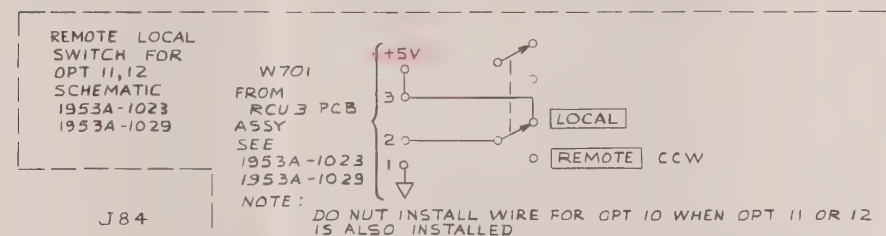
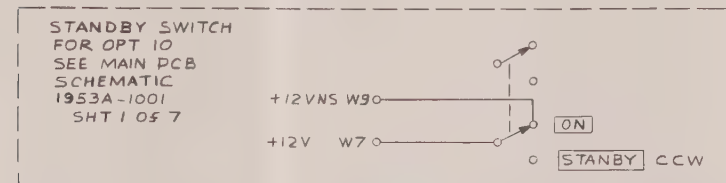
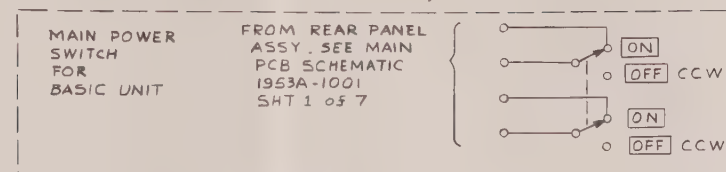


Figure 8-1. Main PCB (1953A-1001) (Sheet 8 of 8)

CONNECTIONS FOR S101 (PART OF R102)



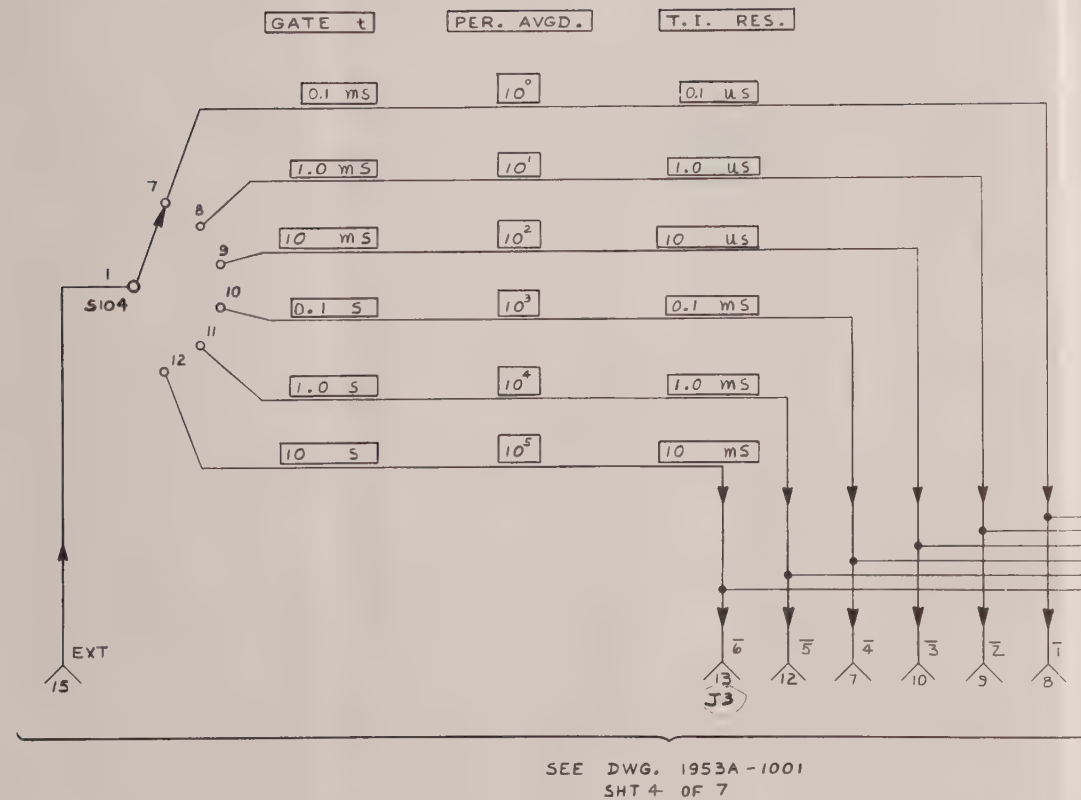
NOTES:

- U113 MAY BE REPLACED BY SEVEN 100 Ω 1/4 W, 5% C.C., DISCRETE RESISTORS P/N 147926
- SEGMENT INDICATION



Figure 8-2. Display PCB Assembly (1953A-1002)

RANGE SWITCH



NOTE:

U301 MAY BE REPLACED BY 13 5K6 DISCRETE RESISTORS.

FUNCTION SWITCH

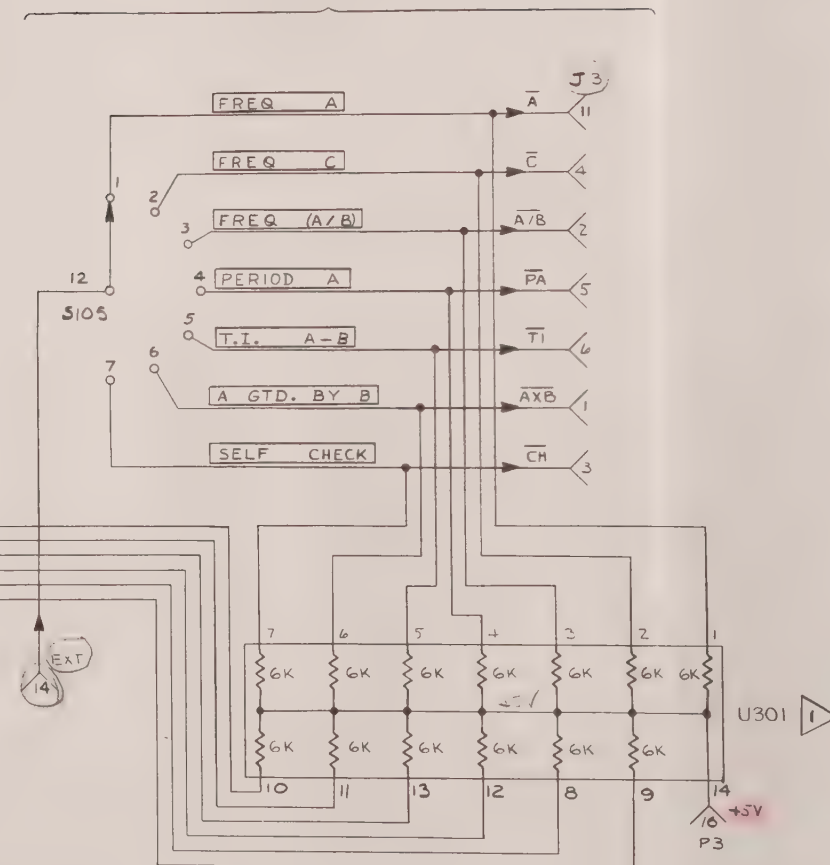
SEE DWG. 1953A-1001
SHT 3 OF 7

Figure 8-3. Switch PCB Assembly (1953A-1003)

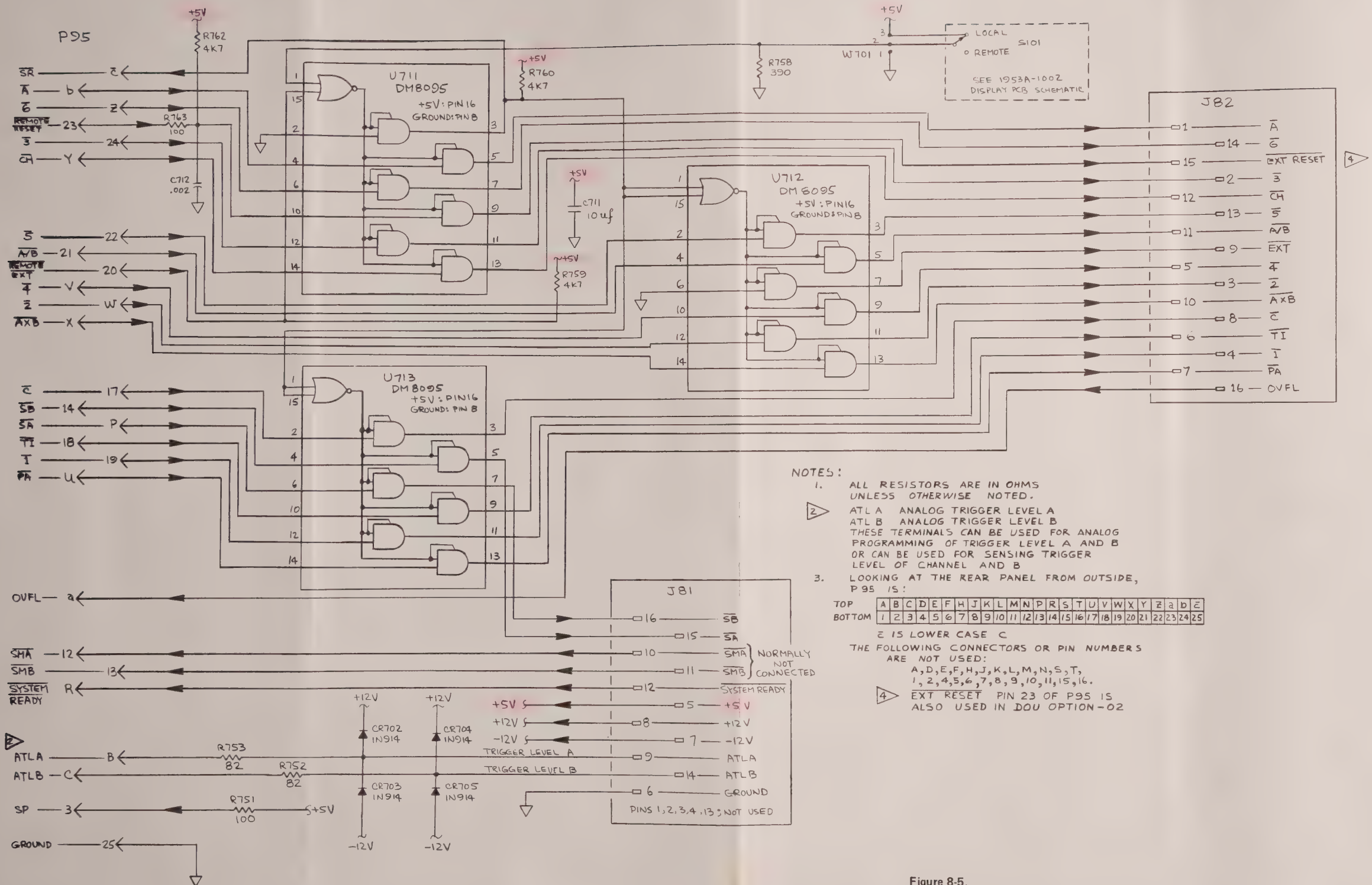


Figure 8-5.
Remote Control Unit Basic PCB Assembly (1953A-1029)

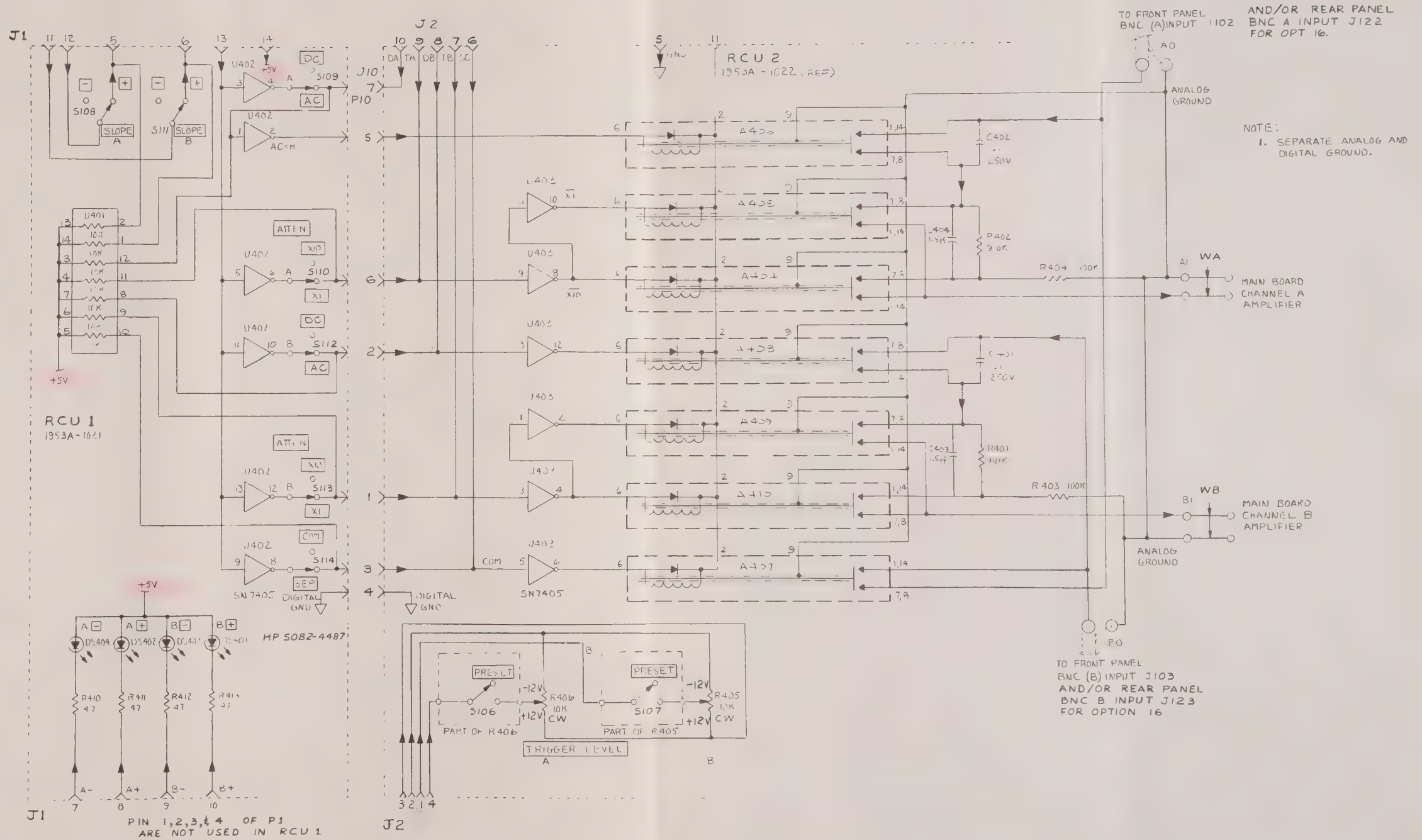
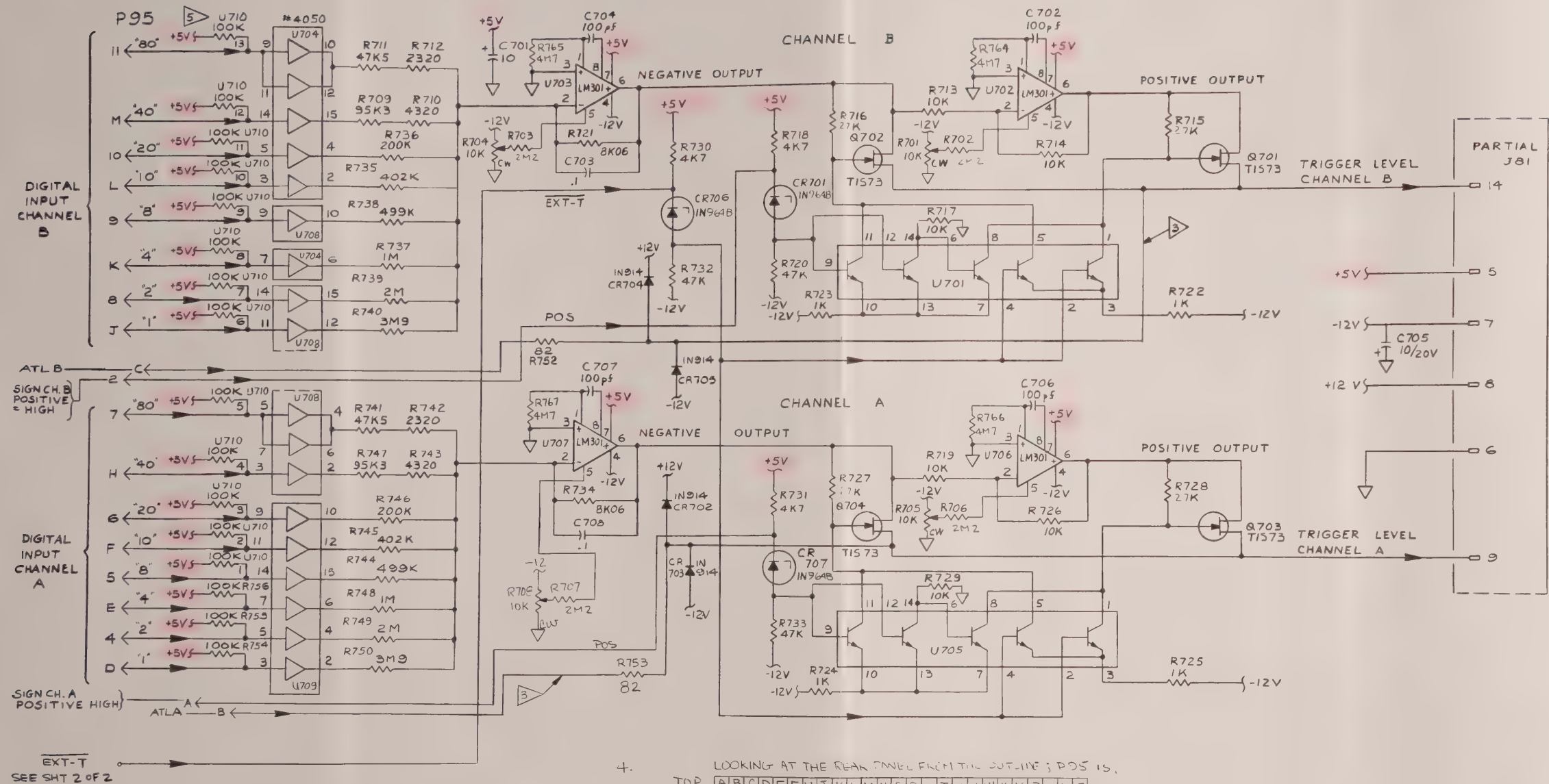


Figure 8-6.
Remote Control Unit 1 & 2 PCB Assemblies (1953A-1021)



NOTES:

1. ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE NOTED.
3. ATLA (ANALOG TRIGGER LEVEL A) ATLB (ANALOG TRIGGER LEVEL B) THESE TERMINALS CAN BE USED FOR ANALOG PROGRAMMING OF TRIGGER LEVEL A AND B OR CAN BE USED FOR SENSING TRIGGER LEVEL OF CHANNELS A AND B.

4. LOOKING AT THE REAR PANEL FROM THE OUTLINE; POS IS

TOP	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25																						
BOTTOM	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

Z IS LOWER CASE C

5. U710 CAN BE SUBSTITUTED BY 13 DISCRETE 100K 1/4W 5% RESISTORS.

6. EXT RESET PIN 23 OF P95 IS ALSO USED IN DOU OPTION-02 (SEE SHT 2 OF 2)

Figure 8-7.
Remote Control Unit 3 (1953A-1023) (Sheet 1 of 2)

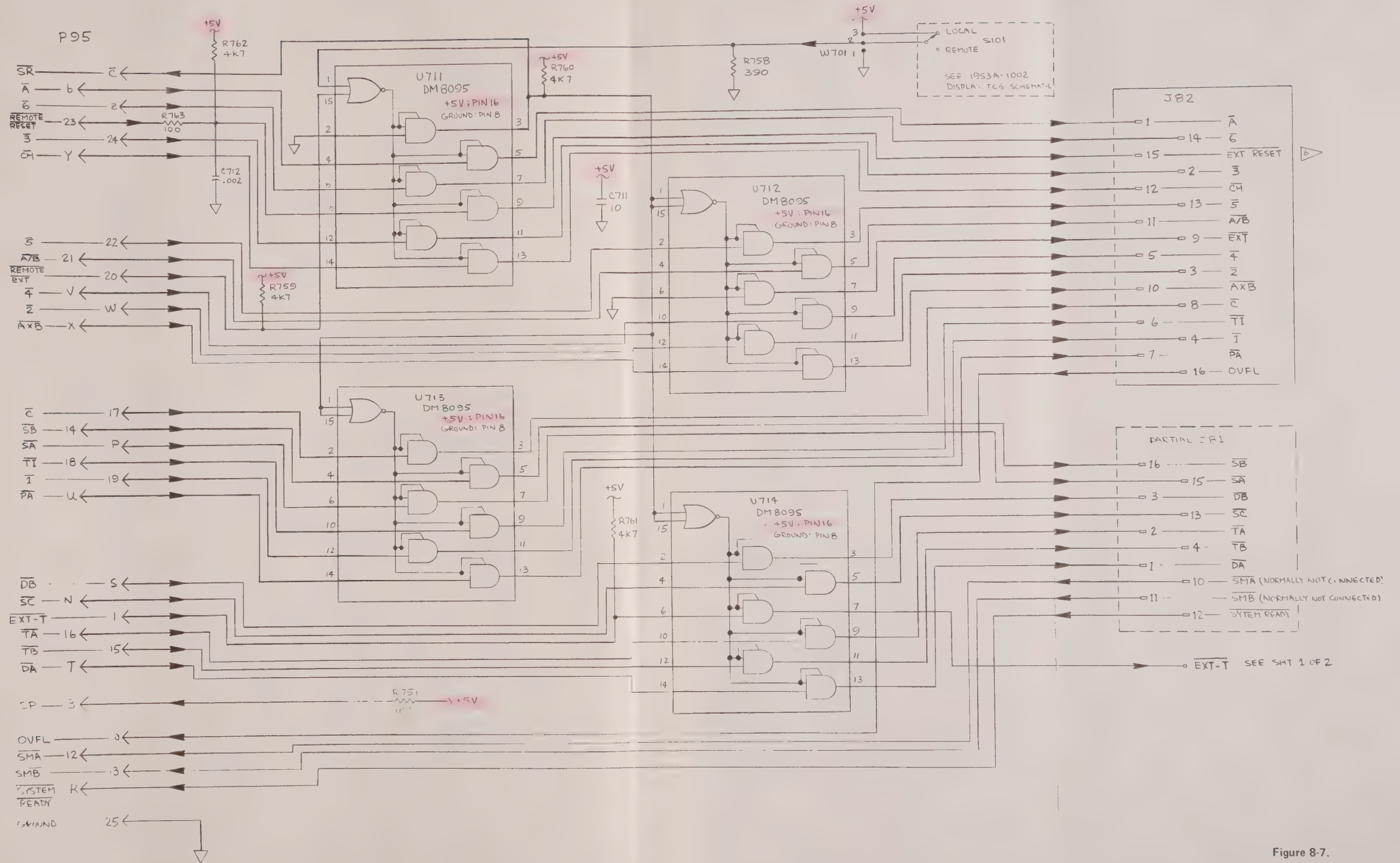


Figure 8-7.
Remote Control Unit 3 (1953A-1023) (Sheet 2 of 2)

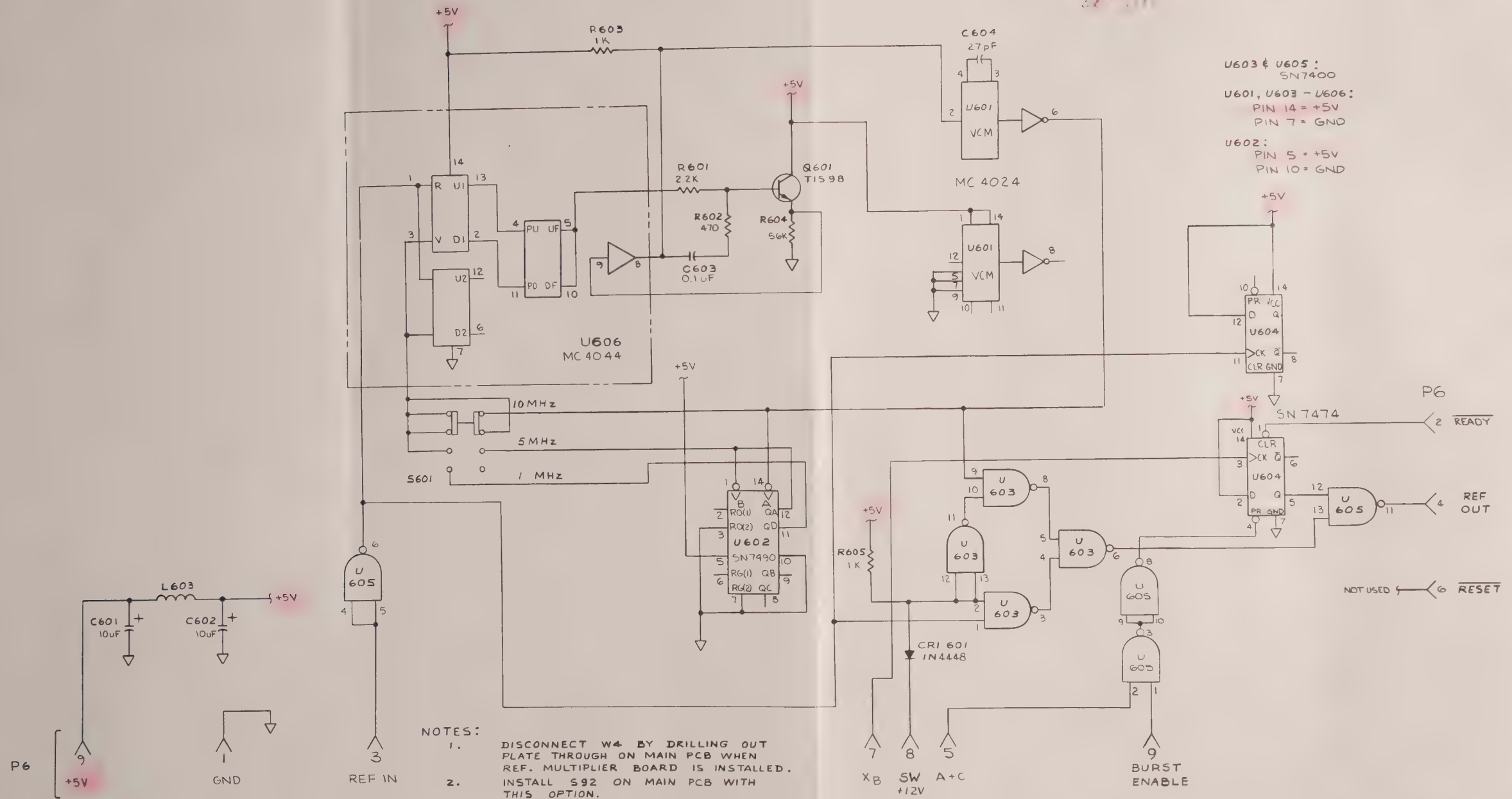


Figure 8-8. Multiplier PCB Assembly (1953A-1033)

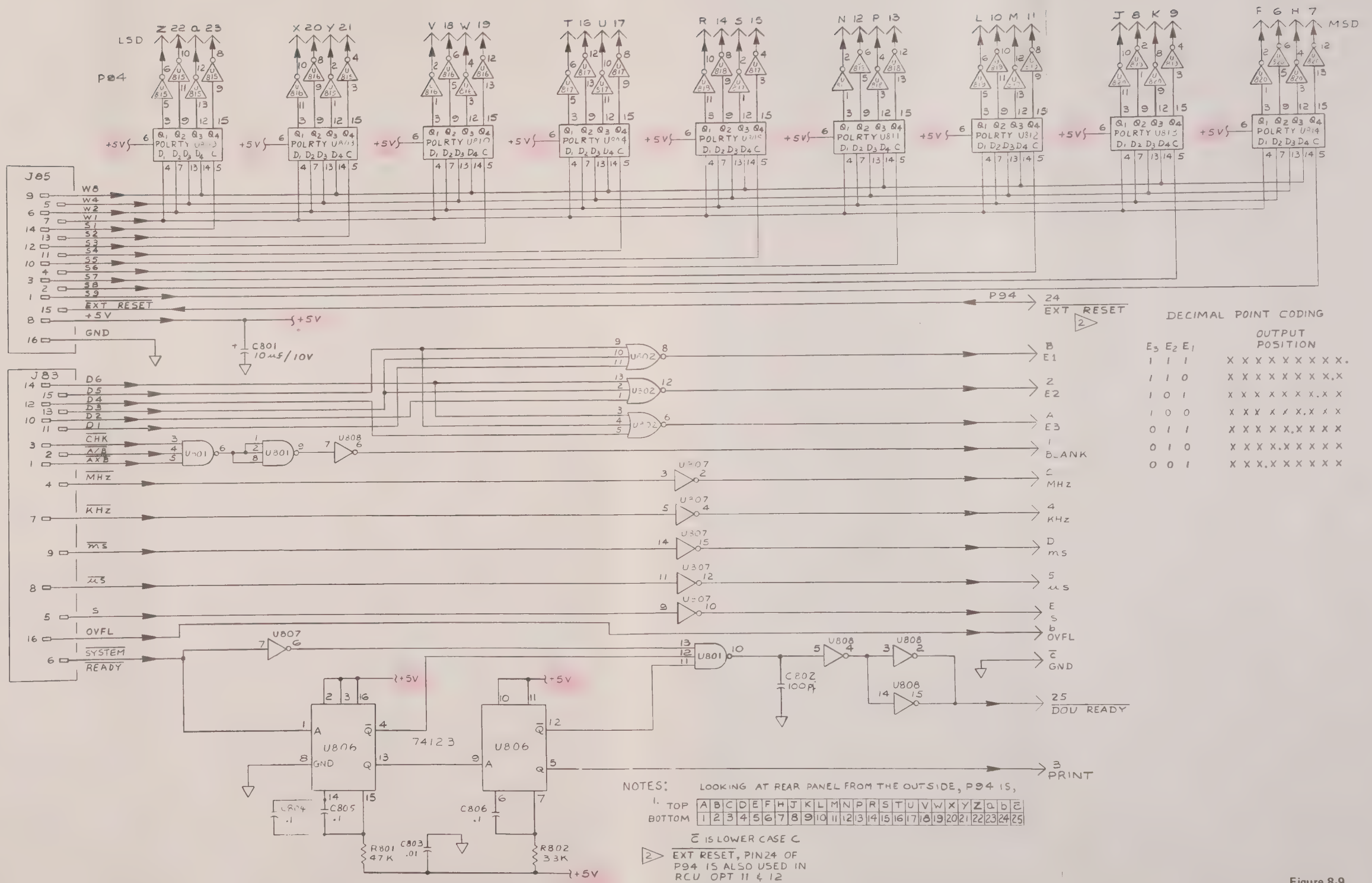
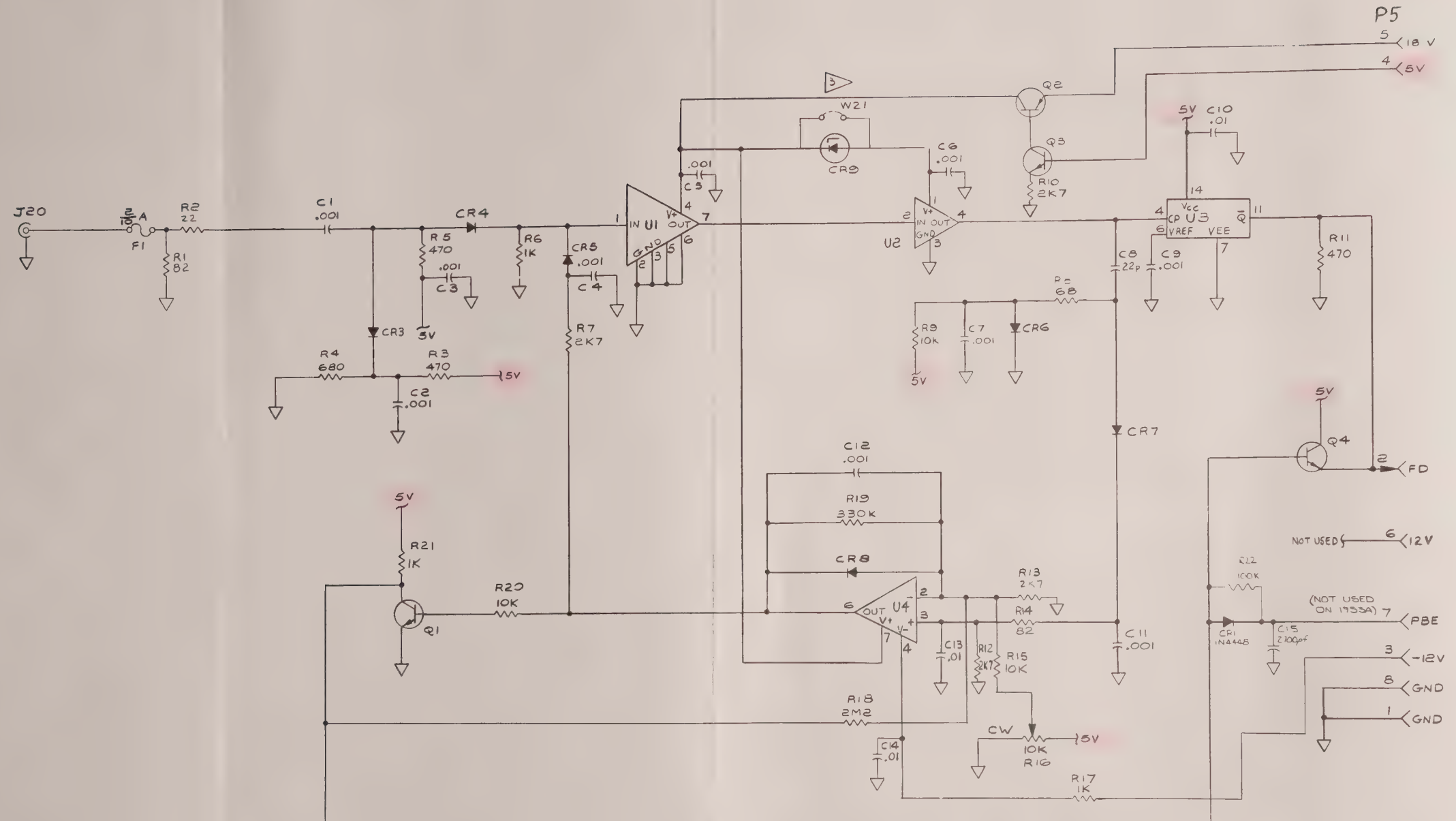


Figure 8-9.
Data Output Unit PCB Assembly (1953A-1025)



NOTES:

- NOTES:
1. ALL RESISTORS ARE IN OHMS, $\frac{1}{4}$ W, 5% CC. UNLESS OTHERWISE NOTED.
 2. ALL CAPACITORS ARE IN MICROFARADS, UNLESS OTHERWISE NOTED.
3. NORMAL U2 IS GPD 402, IF GPD 603 IS USED INSTALL JUMPER WIRE ACROSS W2!

Figure 8-10.
Prescaler PCB Assembly 520 MHz (1953A-1026)

NOTES:

1. ALL RESISTORS ARE IN OHMS, $\frac{1}{4}W$, 5% C.C. UNLESS OTHERWISE NOTED.
 2. ALL CAPACITORS ARE IN MICROFARADS, UNLESS OTHERWISE NOTED.
 3. INSTALL C12 FOR -14 OPTION ONLY.
 4. 1953A-102B 1.25 GHZ PRESCALER SCHEMATIC
5. U2 SELECTED FOR 1.25 GHZ PRESCALER

Figure 8-11
Prescaler PCB Assembly 1 GHz and 1.25 GHz
(1953A-1027/1028)

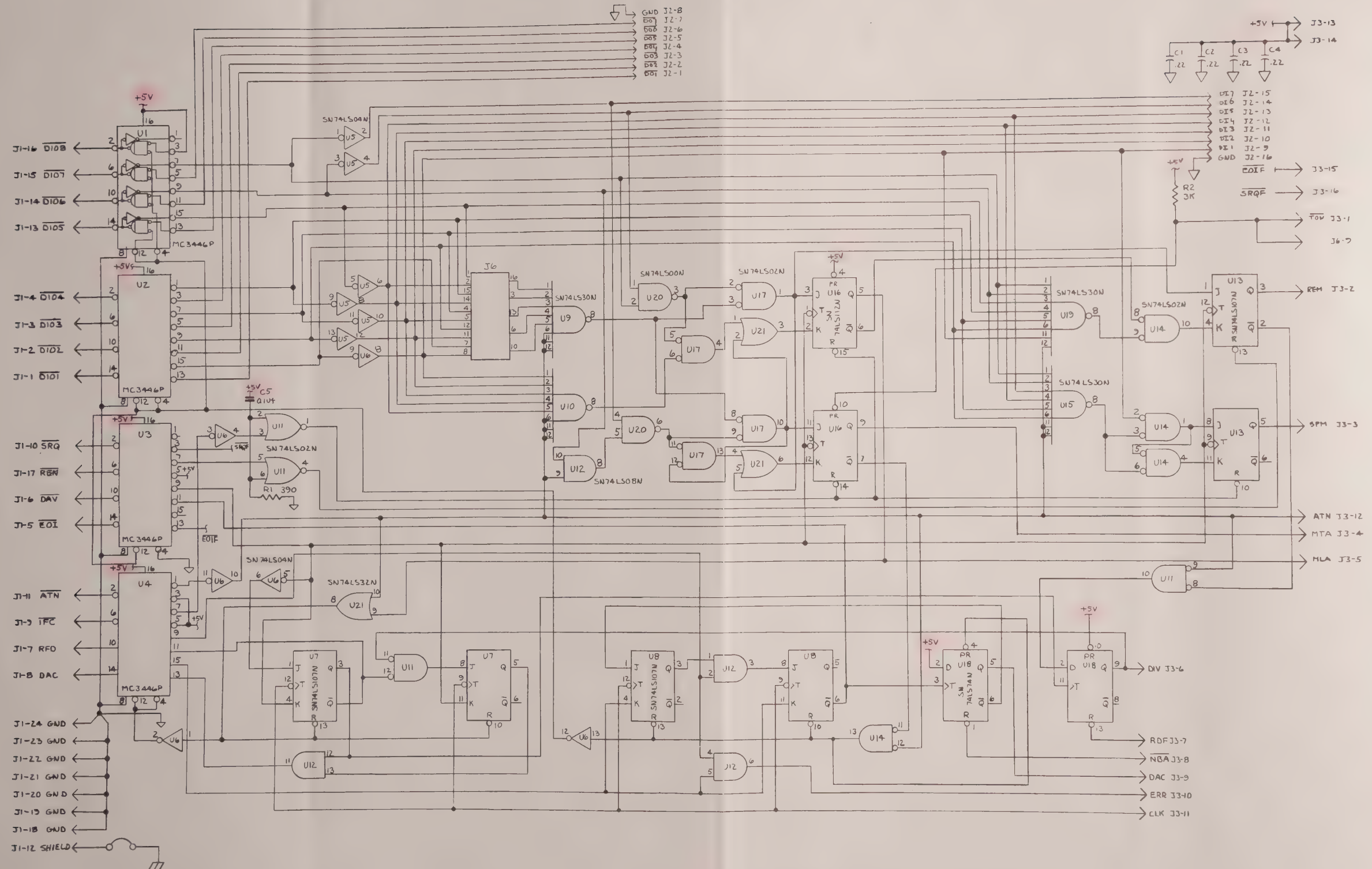
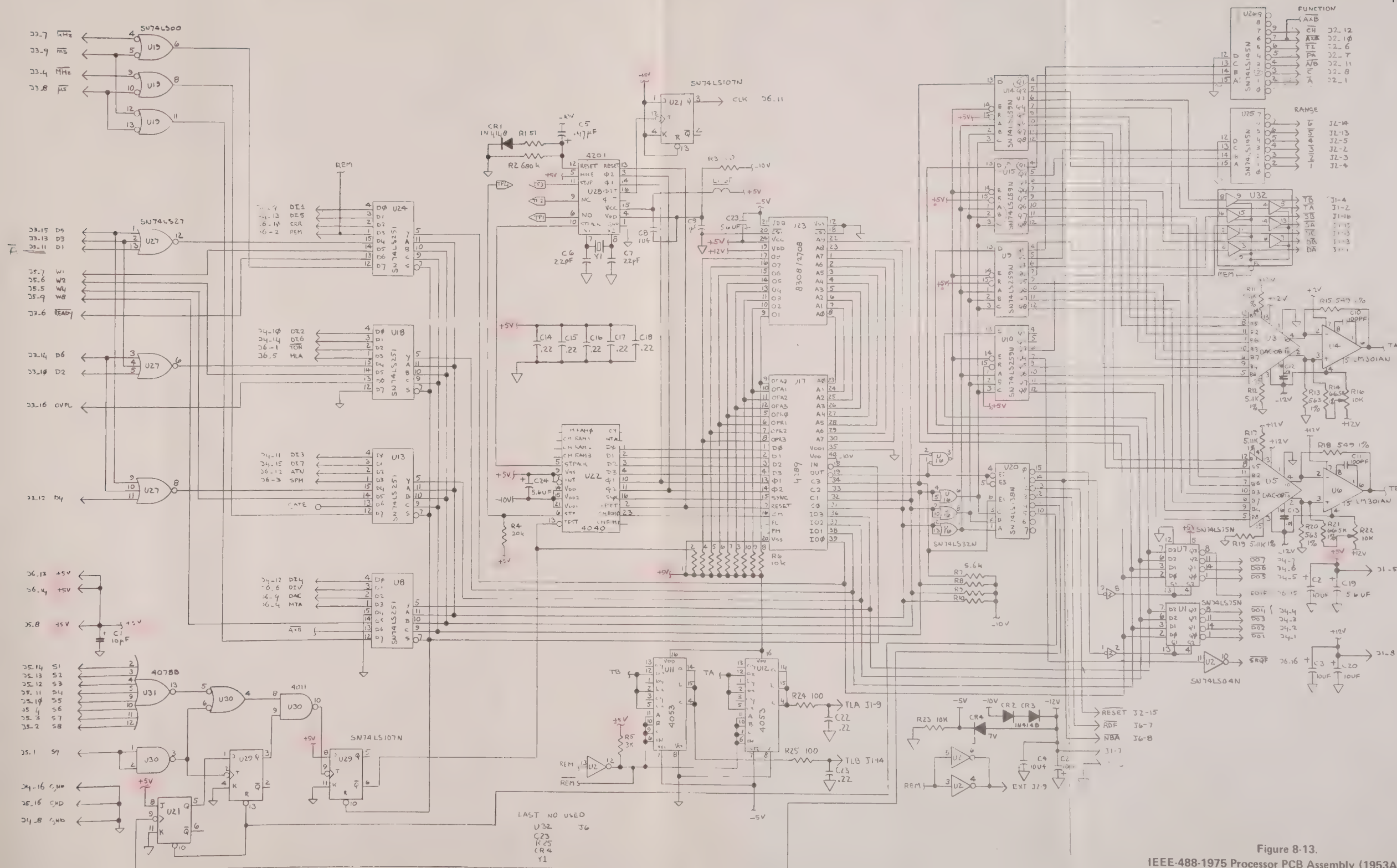


Figure 8-12.
IEEE-488-1975 Interface PCB Assembly (1953A-1040)



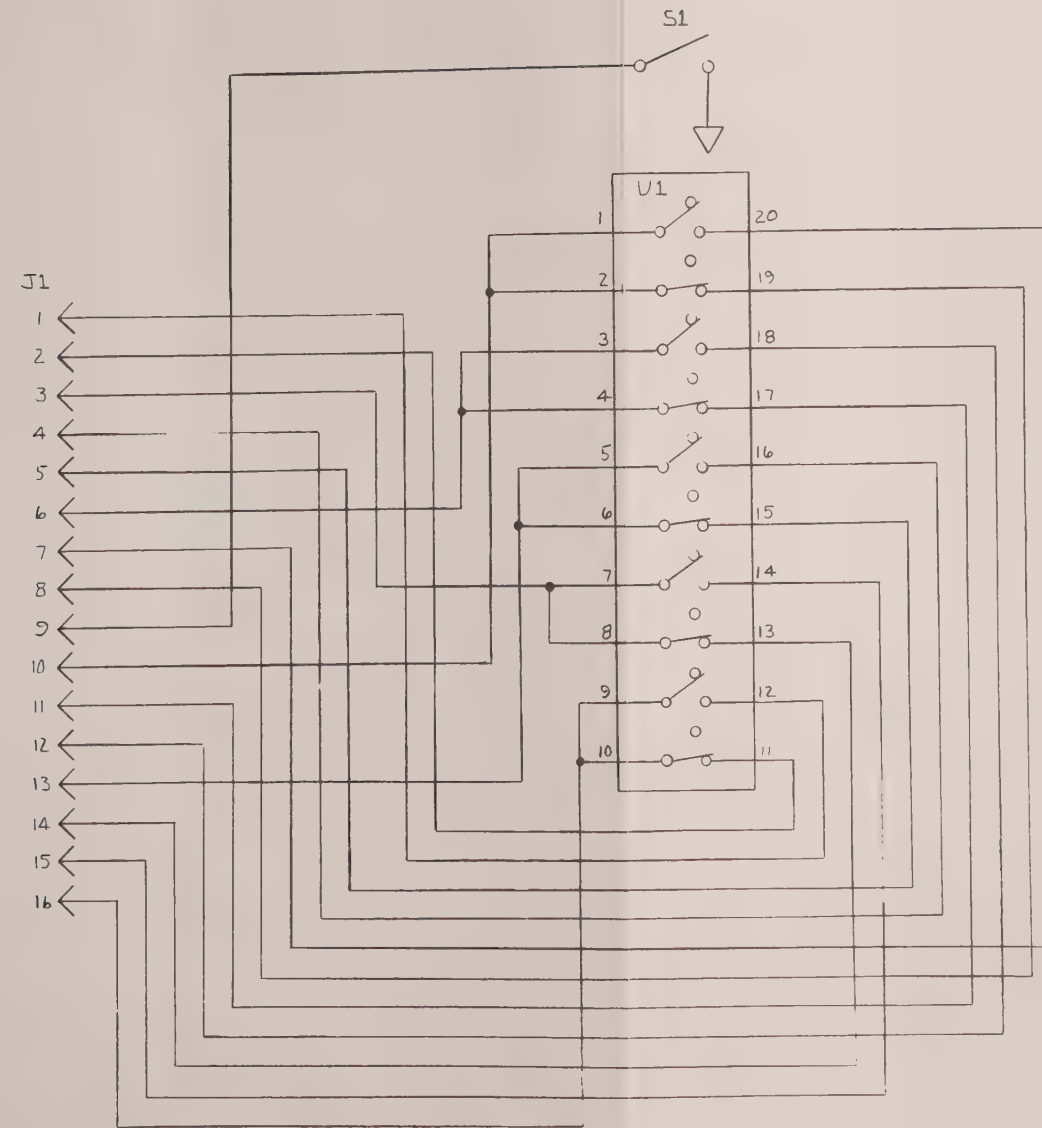


Figure 8-14.
IEEE-488-1975 Switch PCB Assembly (1953A-1042)

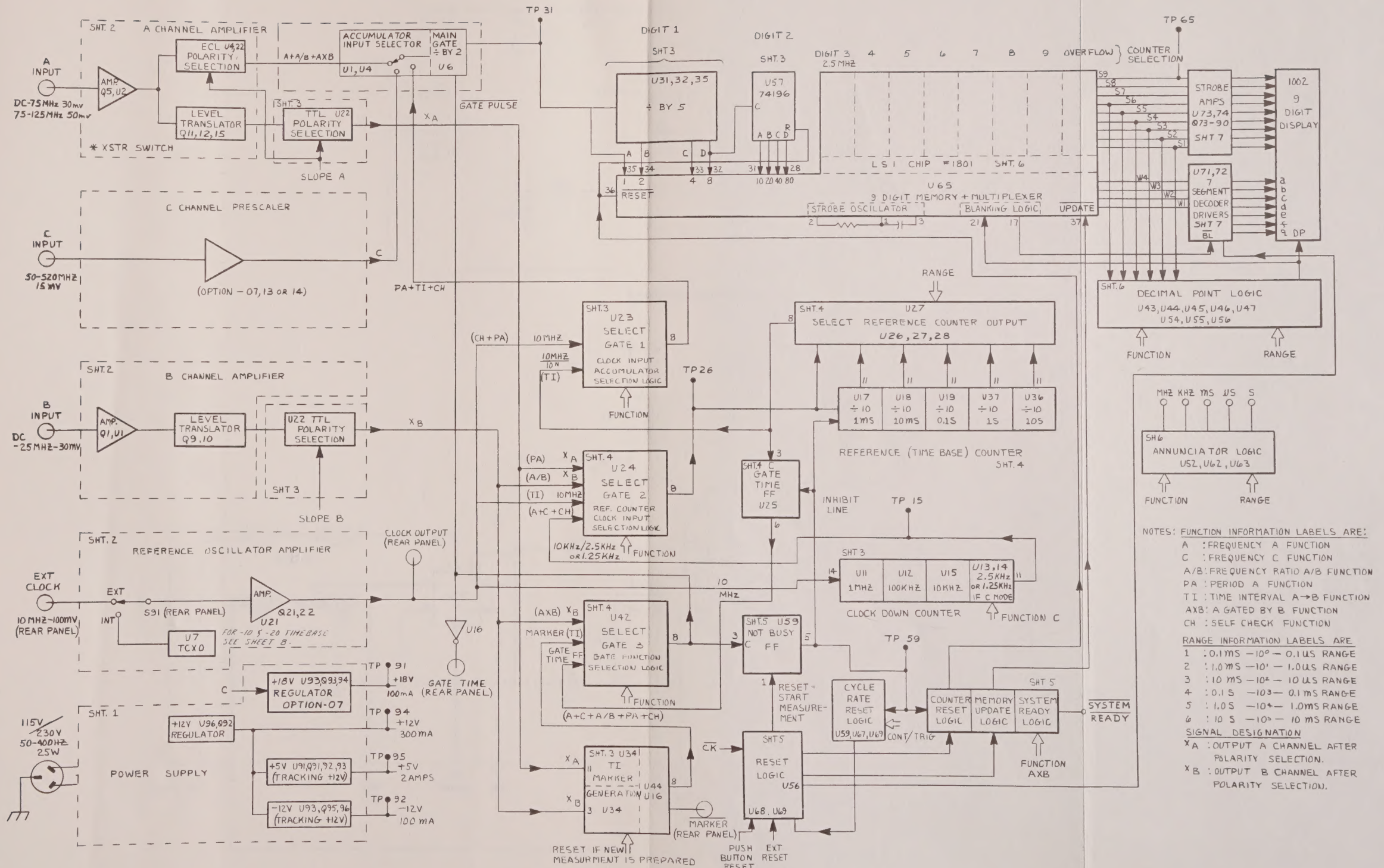
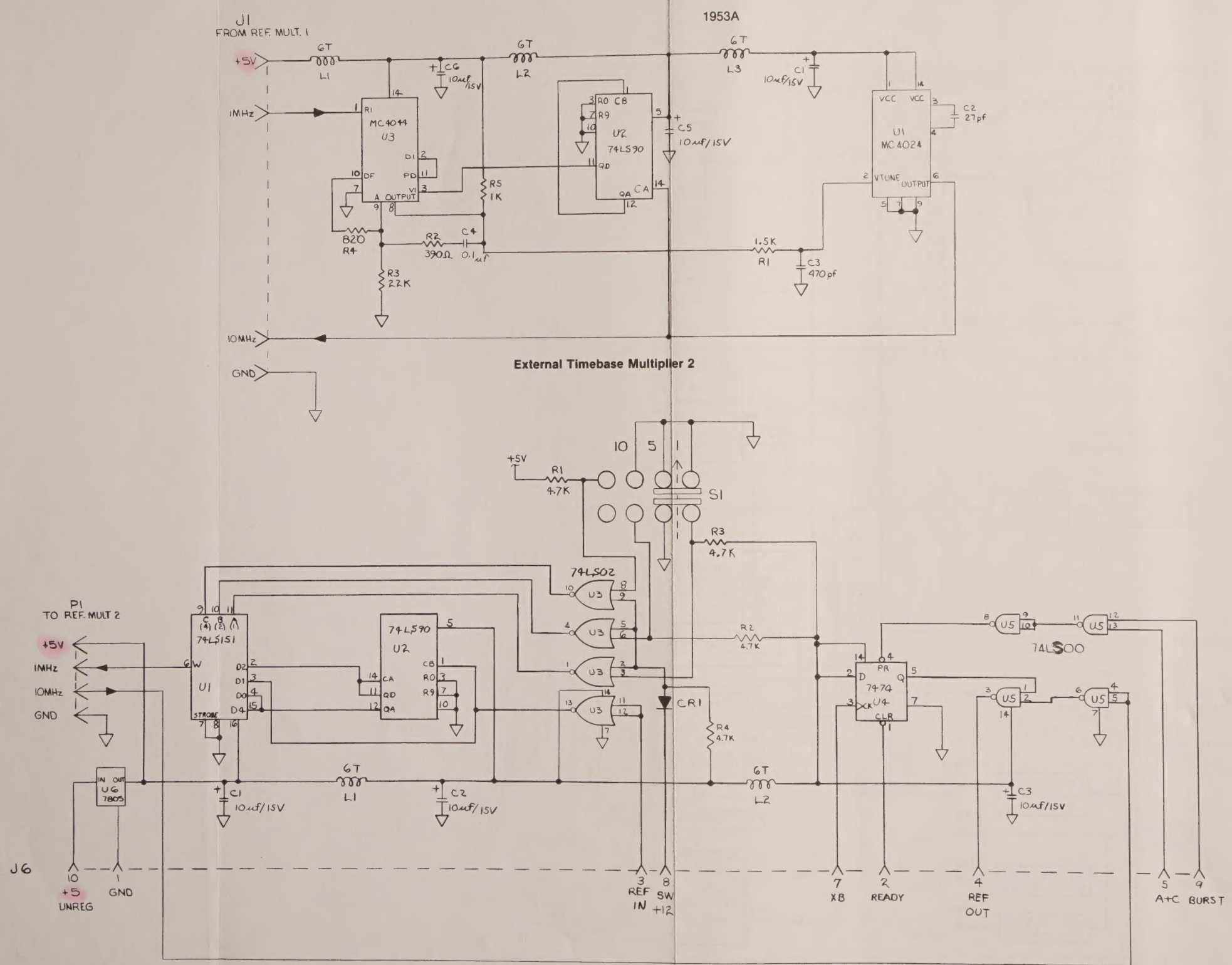


Figure 8-15. Block Diagram 1953A (1953A-1000)



External imebase Multiplier 1

Figure 8-16. External Timebase Multiplier —05 Option (1953A-1034/1035)



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